Standard Product

PCI Reset and Clock Requirements UT699/699E/700 LEON 3FT

Product Advisory

Cobham.com/HiRel

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Table 1: Cross Reference of Applicable Products

PRODUCT NAME	MANUFACTURER PART NUMBER	SMD #	DEVICE TYPE	INTERNAL PIC NUMBER
UT700 LEON	UT700	5962-13238	All	WQ03
UT699E LEON	UT699E	5962-13237	All	WQ01
UT699 LEON	UT699	5962-08228	All	WG07

*** PIC = Product Identification Code**

1.0 Overview

The Leon 3FT microprocessor system-on-chip includes a PCI core that can be configured for 32-bit, 33MHz operations. The PCI core requires proper initialization even when PCI is **NOT** utilized. If proper initialization requirements are not met, the PCI core can lock up the internal AMBA bus in some instances causing the entire processor to lock up. This lockup condition is identified by the processor performing a single access to PROM at address 0x0 following the de-assertion of $\overline{\text{RESET}}$ with no subsequent PROM accesses occurring. This advisory explains the requirements for PCI initialization. The initialization sequence is required during the power-up sequence after which time the PCI core may be utilized normally as described in **Chapter 9.0 PCI Target/Master Unit** of the UT699/UT699E/UT700 Functional Manual. Thereafter, each time power is cycled, the system must perform the initialization sequence. Timing requirements for PCI clock gating are also discussed.

2.0 PCI Initialization Requirements

2.1 PCI Core Utilized in System

Figure 1 shows the required timing relationship between the PCI clock input and the $\overline{\text{RESET}}$ and $\overline{\text{PCIRST}}$ inputs when the PCI core is utilized. It is assumed that the V_{DD} and V_{DDC} power rails are stable and the SYSCLK input has a valid clock as described in Section 4.1 Power Sequencing and Reset of the Leon 3FT Data

Sheet. Parameters t_{CVPH} and t_{CVRH} are specified in PCI clock cycles and must be met in order to ensure that the PCI state machine is initialized to idle state prior to the execution of code. $\overline{\text{RESET}}$ may be de-asserted after 10 valid PCI clock cycles. There is no timing requirement for $\overline{\text{RESET}}$ relative to $\overline{\text{PCIRST}}$. The PCI core may be held in reset by asserting $\overline{\text{PCIRST}}$ until core utilization is required.

If clock gating is used to reduce power, the PCI clock can be disabled after delaying t_{PLCI} following the assertion of the $\overline{\text{PCIRST}}$. Refer to **Table 2** for a summary of the timing parameters.

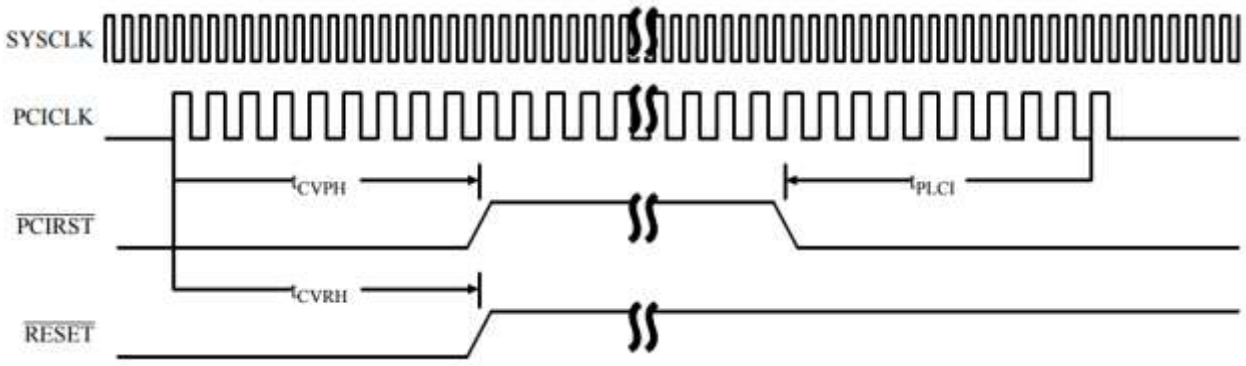

Figure 1: Timing Relationships of Clock and Reset Inputs for PCI Core Utilization

2.2 Initialization of Unused PCI Core

Figure 2 shows the required timing relationship between the PCI clock input and $\overline{\text{RESET}}$ when the PCI core is not utilized. It is assumed that the V_{DD} and V_{DDC} power rails are stable, and that the SYSCLK input has a valid system clock per Section 4.1 Power Sequencing and Reset of the Leon 3FT Data Sheet. The critical timing parameter is t_{CVRH} which must be met in order to ensure that the PCI state machine is initialized to idle state. $\overline{\text{RESET}}$ may be de-asserted after 10 valid PCI clock cycles. The PCI clock input may be permanently tied low or high immediately following the rising edge of $\overline{\text{RESET}}$. Since PCI is not being used, $\overline{\text{PCIRST}}$ is permanently tied to V_{SS}.

Refer to **Table 2** for a summary of critical and recommended timing parameters.

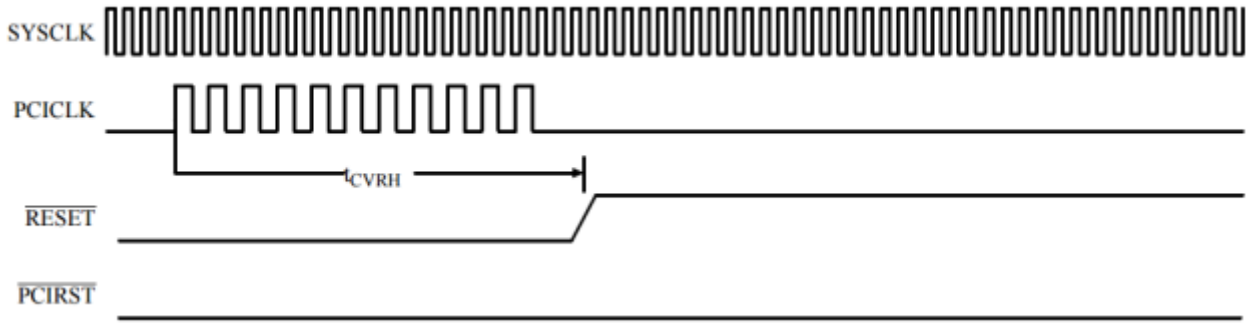

Figure 2: Timing Relationships of Clock and Reset Inputs for Unused PCI Core

2.3 Timing Summary

The following table summarizes the required and recommended timing parameters to ensure proper PCI core and system operation

Table 2: Summary of Timing Parameters

Symbol	Description	Min	Max	Units
t_{CVRH}	PCICLK↑ to $\overline{\text{RESET}}$ de-assertion	10	--	PCI clocks
t_{CVPH}	PCICLK↑ to $\overline{\text{PCIRST}}$ de-assertion	10	--	PCI clocks
t_{PLCI}	$\overline{\text{PCIRST}}$ assertion to PCICLK invalid	10	--	PCI clocks

REVISION HISTORY

Date	Rev. #	Author	Change Description
06/21/2011	1.0.0	--	Initial Release
05/26/2017	1.0.1	MTS	Include UT699E and UT700

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