

**Cobham (formerly Aeroflex)
LEON Manual
Edits since March 11, 2010**

Edits made March 11, 2010

Chapter 1.0, Section 1.2 Table 1 - Added 'Version' column with values AHBSTAT – Changed function statement to 'AHB <u>status</u> register' Added underscore to CAN_OC Added PCIARB line	Page 10
Chapter 1.0, Section 1.6.2 Changed third sentence of paragraph to read, 'See Section <u>17.0</u> for more details.'	Page 16
Chapter 2, Section 2.2.9 Removed last sentence – 'The external error signal will be asserted.'	Page 24
Chapter 3, Section 3.16 Replaced Figure 20	Page 52
Chapter 3, Section 3.16 Replaced Figure 21	Page 53
Chapter 3, Section 3.16 Replaced Figure 22	Page 54
Chapter 3, Section 3.16 Replaced Figure 23	Page 55
Chapter 3, Section 3.16 Replaced Figure 26	Page 58
Chapter 3, Section 3.16 Replaced Figure 27	Page 59
Chapter 3, Section 3.16 Replaced Figure 28	Page 60
Chapter 6, Section 6.4.4 Changed address on UARTSCR Scaler Register to 0x <u>8000010C</u>	Page 73
Chapter 9, Section 9.8 Added new paragraph to Section 9.8 and changed Section 9.8 to Section 9.9. Changed Section 9.9 to Section 9.10.	Page 93

Chapter 11, Section 11.1 Page 99
Changed the first sentence in the first paragraph to read, ‘.....interfaces, each consisting of a GRSPW core.’

Chapter 11, Section 11.2, Subsection 11.2.1 Page 100
Fifth sentence in second paragraph added parentheses around ‘N-Chars’.

Chapter 11, Section 11.2, Subsection 11.2.1 Page 100
Sixth sentence in second paragraph added parentheses around ‘32-bits wide by 16 deep’. Changed wording to read, ‘The AHB FIFOS are 64 Bytes (32-bits wide by 16 words deep).’

Chapter 11, Section 11.2, Subsection 11.2.1 Page 100
First sentence in fourth paragraph changed to read, ‘Each GRSPW core is controlled through eleven.....’

Chapter 11, Section 11.2, Subsection 11.2.2 Page 100
First sentence in second paragraph added, ‘(Does not apply for open packet mode).’

Chapter 11, Section 11.2, Subsection 11.2.2 Page 100
Third sentence in fourth paragraph added a new sentence to read, ‘It is treated as ID (0x00) with zero value data bytes.’

Chapter 11, Section 11.3, Subsection 11.3.1 Page 101
First sentence in fifth paragraph changed to read, ‘.....allowed to send link (characters (L-Char)).’

Chapter 11, Section 11.3, Subsection 11.3.1 Page 101
Second sentence in fifth paragraph changed to read, ‘L-Char’s.....’

Chapter 11, Section 11.4, Subsection 11.4.4 Page 104-105
Table 76 – Removed ‘(Address Offset=0x0) in table title.
Removed the ‘Reset State’ column in table.

Chapter 11, Section 11.4, Subsection 11.4.4 Page 105
Figure 82b – Added ‘Word 1’ after ‘Descriptor’ in the table title.

Chapter 11, Section 11.4, Subsection 11.4.4 Page 105
Table 77 –
Removed ‘(Address Offset=0x4) in table title.
Removed the ‘Reset State’ column in table title.

Chapter 11, Section 11.5, Subsection 11.5.4 Page 108
In Figure 83a, changed bit number 16 to an ‘H’
In Figure 83a, changed bit number 17 to ‘DC’

Chapter 11, Section 11.5, Subsection 11.5.4 Page 108-109
Table 78 –
Changed bit numbers in the first row to read, ‘31-18’.
Changed bit name in bit number 16 to ‘HC’.
Added new description to bit number 16.
Added bit number 17.
Added description to bit number 17.
Removed ‘Reset State’ column in table.

Chapter 11, Section 11.5, Subsection 11.5.4 Table 79 – Removed ‘Reset State’ column.	Page 109
Chapter 11, Section 11.5, Subsection 11.5.4 Table 80 – Removed ‘(Address Offset=0x8) in table title. Removed ‘Reset State’ column in table.	Page 109
Chapter 11, Section 11.5, Subsection 11.5.4 Table 81 – Removed ‘(Address Offset=0xC) in table title. Removed ‘Reset State’ column in table.	Page 110
Chapter 11, Section 11.8 Table 85 – Added missing values to the ‘Reset State’ column for bit numbers 31, 30, 29, 28-18, 16, 15-12, 9, 8, 7, and 2.	Page 118-119
Chapter 11, Section 11.8 Table 86 – Added missing values to the ‘Reset State’ column for bit numbers 31-24, 20-9, and 5.	Page 120
Chapter 11, Section 11.8 Table 87 – Added missing values to the ‘Reset State’ column for bit numbers 31-8.	Page 122
Chapter 11, Section 11.8 Table 88 – Added missing values to the ‘Reset State’ column for all bit numbers.	Page 122
Chapter 11, Section 11.8 Table 89 – Added missing values to the ‘Reset State’ column for all bit numbers.	Page 122
Chapter 11, Section 11.8 Table 90 – Corrected spelling for ‘Description’ in table title. Added missing values to the ‘Reset State’ column for bit number 31-8. Added description to bit number 5-0.	Page 122
Chapter 11, Section 11.8 Table 91 – Added missing values to the ‘Reset State’ column for all bit numbers.	Page 122
Chapter 11, Section 11.8 Table 92 – Added missing values to the ‘Reset State’ column for bit number 31-13, 12, 4, 3, and 2.	Page 124-125
Chapter 11, Section 11.8 Table 93 –	Page 126

Added missing values to the ‘Reset State’ column for all bit numbers.

Chapter 11, Section 11.8 Page 126
Table 94 –

Added missing values to the ‘Reset State’ column for all bit numbers.

Chapter 11, Section 11.8 Page 126
Table 95 –

Added missing values to the ‘Reset State’ column for all bit numbers.

Chapter 13, Section 13.2, Subsection 13.2.16 Page 154
Table 137 –

Added bit name to bit number 15-0.

Chapter 15, Section 15.3 Page 167

Changed sentence to read, ‘The STET....’

Added spaces between all of the words in this sentence.

Removed second sentence.

Chapter 15, Section 15.3 Page 167
Table 155 –

Changed table title to read, ‘Description of STET....’

Removed extra spaces in title.

Chapter 15, Section 15.3 Page 167

Figure 132 –

Changed figure title to read, ‘DEBUG....’

Chapter 15, Section 15.3 Page 167

Table 156 –

Changed figure title to read, ‘Description of DEBUG....’

Edits made January 4, 2012

Chapter 1.0, Section 1.2 Page 10

Added underscore to CAN_OC

Chapter 2.0, Section 2.1, Subsection 2.1.1 Page 17

Changed second sentence of paragraph to read, ‘The integer unit has eight register windows providing a....’

Chapter 2.0, Section 2.2, Subsection 2.2.14 Page 26

Changed first sentence of paragraph to read, ‘....implemented with a Bose-Chauduri-Hooquenghem....’

Chapter 2.0, Section 2.4, Subsection 2.4.5 Page 30

Figure 8 -

Changed figure title to read, ‘....Layout for 4kB per Way....’

Chapter 2.0, Section 3.5

Page 40-41

Figure 12 –

Changed labels in the ‘Memory Controller’ box: First label to read, ‘*_ROMS[1:0]’; Fourth and fifth label to read, ‘*_RAMS[4:0]’; Sixth label to read, ‘RWE[3:0]’

Added note to read, ‘*When the EDAC is enabled in 8-bit bus mode, only the first bank select (RAMS[0], ROMS[0] can be used.’

Figure 14 –

Changed labels in the ‘Memory Controller’ box: First label to read, ‘ROMS[1:0]’; Fourth and fifth label to read, ‘RAMS[4:0]’

Chapter 3.0, Section 3.10

Page 43

Changed fifth sentence of third paragraph to read, ‘...data memory while the top 20% is used....’

Chapter 3.0, Section 3.16

Page 56-57

Figure 24 –

Changed figure title to read, ‘...Write Cycle on a 32-bit bus’

Figure 25 -

Changed figure title to read, ‘...SRAM 16-bit write cycle on a 16-bit bus’

Added note to read, ‘*For 8-bit bus architectures, ADDR[27:0] and Data [31:24] and RWE[3] are used.’

Chapter 3.0, Section 3.16

Page 61

Figure 29 –

Changed label on next to the last bar to read, ‘*_ADDR[27:2]’

Changed label on the last bar to read, ‘*_DATA[31:0]’

Added note to read, ‘*For 16-bit I/O bus configurations ADDR[27:1] and Data [31:16] are used. For 8-bit I/O bus configurations ADDR[27:0] and Data[31:13] are used.’

Chapter 11.0, Section 11.5, Subsection 11.5.4

Page 108

Table 78 –

Description for Bit Number 17 added, ‘Data CRC’

Changed second paragraph to read, ‘Append CRC....’

Changed Bit Name for Bit Number 16 to read, ‘HC’

Chapter 11.0, Section 11.8

Page 119

Table 85 –

Added an ‘X’ to Reset State for Bit Number 7.

Chapter 13.0, Section 13.3

Page 155

Table 138 –

Changed Bit Name to read, ‘Address LSB’.

Chapter 15.0, Section 15.3

Page 168

Table 157 –

Changed Description for Bit Number 2, third sentence, to read, ‘Read only.’

Edits made January, 2012

Chapter 2.0, Section 2.4, Subsection 2.4.11 Page 34
Fourth sentence, added space between 'register' and '%gl'.
Fifth sentence, added space between 'of' and '%gl'.

Chapter 3.0, Section 3.5 Page 40
Figure 12 –
Changed note to read, '...(RAMS[0], ROMS[0])....'

Chapter 3.0, Section 3.9, Subsection 3.9.3 Page 42
Added line space between Subsection 3.9.3 and Subsection 3.9.4

Chapter 3.0, Section 3.9, Subsection 3.9.6 Page 43
Changed second sentence to read, '....internal system clock....'

Chapter 3.0, Section 3.10 Page 43
Changed third paragraph, third sentence, removed comma after address.

Chapter 3.0, Section 3.16 Page 61
Changed first sentence of note to read, '....ADDR[27:1]...'.
Changed second sentence of note to read, '....ADDR[27:0]....'.

Chapter 11.0, Section 11.5, Subsection 11.5.4 Page 108
Table 78 –
Changed Description for Bit Number 16 to read, 'Header CRC'.
Changed third sentence of Description for Bit Number 16 - Added an 'l' to 'length'.

Chapter 11.0, Section 11.5, Subsection 11.5.4 Page 110
Table 81 –
Removed '(Address Offset=0xC) in table title.

Chapter 11.0, Section 11.8 Page 124
Table 92 -
Added a '0' to the Reset State column for Bit Number 16.
Changed bit number to 15-13 rather than 13-15.

Chapter 13.0, Section 13.3 Page 155
Table 138 –
Changed Bit Name to Address LSB rather than Address CSB.

Chapter 15.0, Section 15.3 Page 167
Table 156 –
Added '0' to Reset State Column for Bit Number(s) 1 and 0.

Chapter 15.0, Section 15.3 Page 168
Table 157 -
Corrected spelling of the word 'characters' under the Description for Bit Number 4.
Under the Description of Bit Number 2, second paragraph, changed 'Indicated' to 'Indicates'.

Edits made February 16, 2012

Chapter 2.0, Section 2.4, Subsection 2.4.11 Page 34
Third sentence, added an 'r' to register.

Edits made March 1, 2012

Chapter 11.0, Section 11.8 Page 126
Table 95 –
Changed Bit Number to 9-3 from 9-4.
Changed Bit Number 2-0 from 3-0.
Changed Description under Bit Number 9-3, third sentence to read, '....increments to 128.....'

Edits made March 12, 2012

Chapter 3.0, Section 3.14, Subsection 3.14.1 Page 49
Changed Bit Name for Bit Number 9 to 'RE' from 'SE'.
Changed Description for Bit Number 9, first sentence to read, '....SRAM/SDRAM areas'.

Edits made March 20, 2012

Application Notes Page 174
Added total of eight notes to this section.

Edits made April 2, 2012

Chapter 3.0, Section 3.10 Page 43
Added paragraph four to read, 'NOTE: When the EDAC is enabled in 8-bit bus mode, only the first bank select (ROMS[0], RAMS[0]) can be used.'

Chapter 3.0, Section 3.10 and Section 3.11 Page 43
Removed a line space between Section 3.10 and Section 3.11.

Edits made June 20, 2012

Chapter 3.0, Section 3.2
Added PROM access clarification.

Edits made November 1, 2013

Chapter 3.0 Page 57
Changed RWE[3] to RWE[0]

Page 40
Changed RWE[3:0] to RWE[0] in figure 12

Chapter 3.0, section 3.2 Page 39
Changed upper half (0x00000000 to upper half (0x10000000

Chapter 3.0, section 3.14.1, figure 15 Page 45
Changed bit 27-28 from IW to ID

Changed bit 27-28 from IW to ID

Chapter 3.0, section 3.14.1, Table 27 Page 45
Changed bit 27-28 from IW to ID

Chapter 3.0, section 3.14.1, Table 28 Page 47
Removed verbiage “is 2048 when bits [25:23] = 111 Otherwise, the column size is defined as:” from description for bit 21-22

Chapter 3.0, section 3.14.1, Table 28 Page 47
Added verbiage “when bits [25:23] = “111”; 2048 Otherwise” to description for bit 21-22

Chapter 5.0, section 5.2.2, Table 32 Page 66
Changed Interrupt # 4 to 3

Chapter 5.0, section 5.2.2, Table 32 Page 66
Add Interrupt # 4 to 5

Edits made February 1, 2014

Chapter 2.0, section 2.2.7 Page 22
Trace buffer number of lines from 256 to 128

Chapter 2.0, Table 18 Page 33
Bit number 27 reset state from 0 to 1
Bit number 7-4 reworded description
Bit number 3-0 reworded description

Chapter 14, section 14.3 and 14.4 Page 159
Trace buffer number of lines from 256 to 128 Page 160

Edits made February 19, 2016

Table 3.4, bit numbers 17-14 Page 55