

UT32M0R50x

32-bit ARM[®] Cortex[™]-M0+ Microcontroller

Product Brief

Cobham.com/HiRel

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The most important thing we build is trust

KEY FEATURES

- ▶ Operating Voltage
 - Supports single 3.3 V (3.0 V to 3.6 V) supply
- ▶ System
 - 32-bit ARM[®] Cortex[™]-M0+ processor
 - Include nested vector interrupt controller (NVIC)
- ▶ Digital and Communication Peripherals
 - CAN 2.0B Controller
 - UART
 - SPI
 - I2C
 - PWM
 - Watchdog Timer
 - Real Time Clock
 - Configurable GPIO Ports
- ▶ Analog Peripherals
 - 12-bit ADC 100 kps with PGA
 - 16 Single Ended or 8 Differential Channels
 - 1 mA Precision Current Source
 - 12-bit DAC and Analog Voltage Comparator
 - Analog Voltage Comparators
 - On-chip Temperature Sensor
- ▶ Power Control
 - Multiple power modes for low power optimization
 - System clock scalable for low power
 - Power-on-Reset
- ▶ Memory
 - Internal Dual Port SRAM with EDAC+Scrubbing
 - Non-volatile Flash Memory
- ▶ System Clock
 - 50 MHz internal clock factory-trimmed clock
 - Support for external clock source or crystal oscillator
- ▶ Standard Microelectronics Drawing (SMD):
 - *5962-TBD (QML-Q/Q+ Pending)*
- ▶ Package Options:
 - 143-Pin LGA, CGA, BGA (prototype only)

OPERATIONAL ENVIRONMENT

- ▶ Temperature Range: -55°C to +105°C
- ▶ Total Dose : ≥ 50 krad(Si)
- ▶ SEL Immunity

APPLICATIONS

- ▶ Telemetry/System Health Monitoring
- ▶ Data Acquisition
- ▶ SpaceVPX
- ▶ RF Signal Chain

SUPPORT

- ▶ Keil[®] MDK ARM Development Tool Environment

INTRODUCTION

The UT32M0R500 microcontroller utilizes the ARM[®] Cortex[™]-M0+ processor with a 32-bit RISC architecture operating at a 50 MHz frequency. The microcontroller includes a memory protection unit (MPU), embedded memories, with several peripherals including support for CAN 2.0B. For increased design flexibility, the microcontroller includes several analog features such as an analog signal channel with a multiplexed input combined with a programmable gain amplifier and analog-to-digital converter, digital-to-analog converters, analog comparators, and precision current source.

The UT32M0R50x incorporates a variety of power-saving modes to facilitate the design of low-power applications.

For information on the ARM[®] Cortex[™]-M0+ core please refer to the ARM[®] Cortex[™]-M0+ Technical Reference Manual, available from the www.arm.com website.

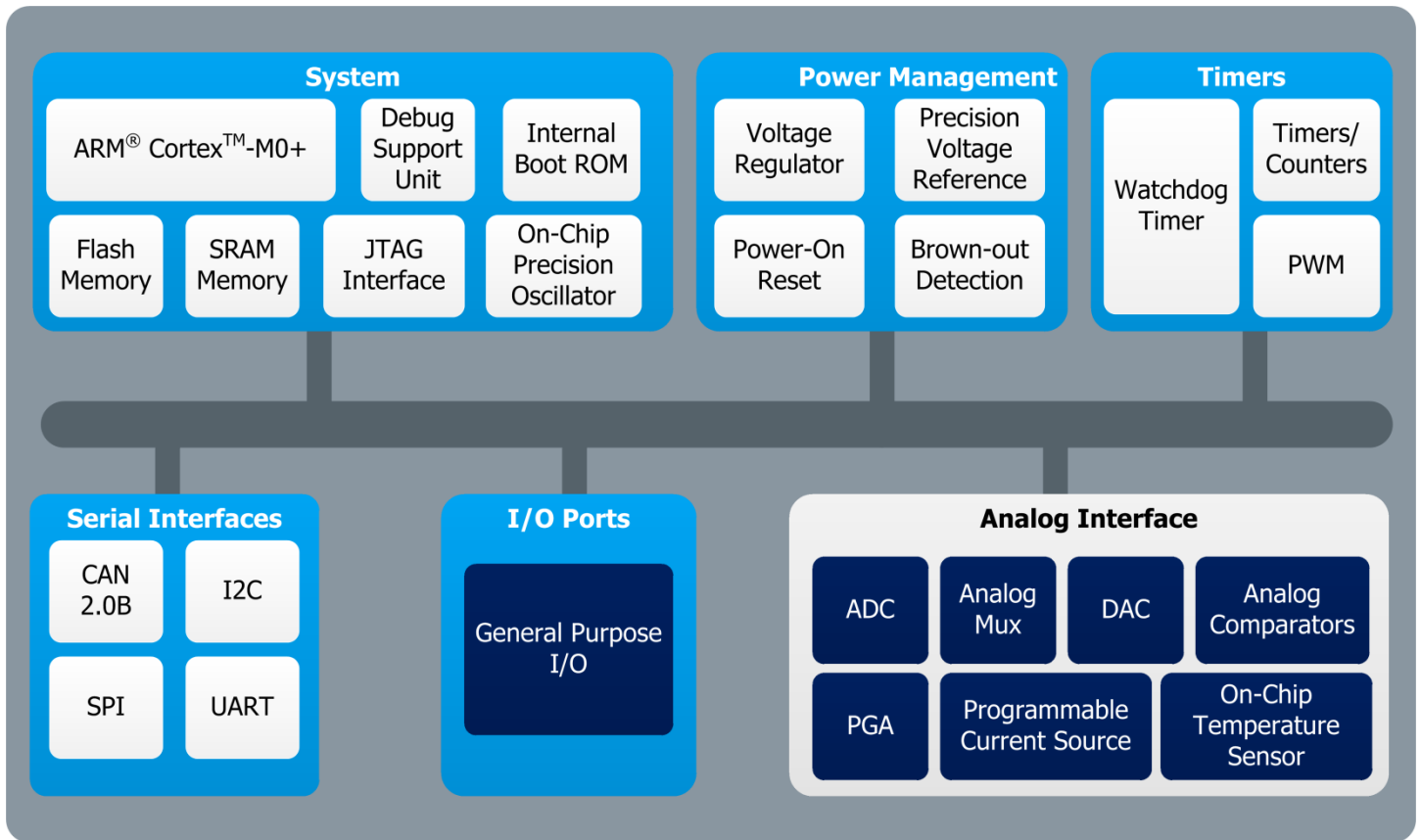


Figure 1: UT32M0R500 Simplified Block Diagram

ARM® Cortex™-M0+ Processor with MPU

The Cortex-M0+ processor is a low-power 32-bit ARM Cortex processor designed for wide range of embedded applications. The Cortex-M0+ is based on highly optimized 32-bit processor core with a x-stage pipeline Von Neuman architecture. The processor has exceptional energy efficiency with a small but powerful instruction set coupled with a hardware single-cycle multiplier and Memory Protection Unit (MPU).

With the use of the ARM core, the UT32M0R500 is compatible with the ARM tools and software.

Table 1: UT32M0R500 Cortex-M0+ Configuration

Features	ARM M0+ Configurable Option	UT32M0R500 Configuration
Interrupts	0 – 32	32
Data Endianness	Little-endian or big-endian	Little-endian
SysTick Timer	Present or absent	Present
Number of Watchpoint Comparators	0, 1, 2	2
Number of Breakpoint Comparators	0 - 4	4
Multiplier	Fast or small	Fast (Single Cycle)
Wakeup Interrupt Controller	Supported or not support	Supported
Vector Table offset Register	Present or absent	Present
Unprivileged/Privileged Support	Present or absent	Present
Memory Protection Unit	Present or absent	Present
Reset All Registers	Present or absent	Present
Debug Configuration	Present or absent	Present
Micro Trace Buffer	Present or absent	Present

Cobham Semiconductor Solutions – Datasheet Definitions

Advanced Datasheet - Product In Development

Preliminary Datasheet - Shipping Prototype

Released Datasheet - Shipping QML & Reduced Hi – Rel

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Cobham Semiconductor Solutions
4350 Centennial Blvd
Colorado Springs, CO 80907

E: info-ams@aeroflex.com
T: 800 645 8862

The logo for Cobham, featuring the word "COBHAM" in a bold, italicized, white sans-serif font against a blue background.