# UTXQ512 SRAM Frequently Asked Questions

**Introduction**:
The UTXQ512 are high-performance CMOS asynchronous static RAMs organized as 512K words by 8 bits. The following are questions frequently asked regarding these devices. Detailed information on these devices can be found in the UTXQ512 Data Sheets.

**Questions and Answers**:

**Question 1**:)

Are the I/O of the 3.3V device compatible (interoperable) at 5V I/O?

*Answer 1*:)

- 5V is not compatible with 3.3 (100ns)
- 3V is not compatible with 5.0 (25ns)

**Question 2**:)

What are the die sizes for the 3.3V as the 5V?

*Answer 2*:)

- 5V UT7Q512 - 250mils x 430mils (100ns) - 32-lead ceramic flatpack
- 3V UT8Q512 - 264mils x 57mils (25ns) - 36-lead ceramic flatpack
- 3V and 5V UT9Q512 - 264mils x 57mils (25ns) - 36-lead ceramic flatpack

**Question 3**:)

Please provide the die size for the UT8Q512, 3.3V dice and the UT7Q512, 5.0V dice.

*Answer 3*:)

264mils x 572mils (see **Figure 2** )

**Question 4**:)

If you cannot immediately provide die maps, please at least describe where the bond pads are on the die, i.e. are they all at the top and bottom (along the short side only), or are there bond pads all around the die on all four sides.

*Answer 4*:)

Bonding on all 4 sides (see **Figures 1** and **2**)

**Question 5**:)

QML-T Flow, what does this offer?

*Answer 5*:)

QCOTS Flow (see the QML T Screening FAQs)
100% Aracor wafer screening

2 test structures per wafer (100% wafers per lot)
2 wafer per lot mapped for assessment of intra wafer variability
Sample Cobalt screening
5 samples per lot (90% probability with 90% confidence level)
Structural analysis
Contact/Via/Poly
QML assembly (Group A, C, E, D3 and D4)
SMD procurement vehicle
Value added
Wafer street cleaning, eliminates pealing metal and shorts
Wafer Lot Assurance
Radiation performance (SEE and Total Dose)
Reliability assessment (Oxide integrity)
Fit Rate target < 10

**Question 6**:)

Do we get 100% visual inspection on the die?

*Answer 6*:)

Yes, Visual per Aeroflex UTMC's QML Q (low magnification)

**Question 7:)**

Is the visual inspection performed Class A for Space.

*Answer 7*:)

Yes, Visual per Aeroflex UTMC's QML Q (low magnification)

**Question 8**:)

Have all the die received 100% electrical probing?

*Answer 8*:)

At room temperature, by die supplier

**Question 9:)**

At what temperature has the die been probed? Ambient and Hot?

*Answer 9*:)

At room, by die supplier, not at hot

**Question 10**:)

Has SEM or Wafer Lot Acceptance been performed on the lot?

*Answer 10*:)

Yes, per Aeroflex UTMC's QML T flow

**Question 11**:)

Will the die all come from the same lot?

*Answer 11*:)

Dependent on volume, all wafer lots will see the same screening.

**Question 12**:)

What is the address access time?

*Answer 12*:)

The address access time for the UT7Q512 is 100ns and the address access time for the UT8Q512 and UT9Q512 is 25ns.

**Question 13**:)

What is the UT7Q512 32 flatpack test socket number and manufacturer's name?

*Answer 13*:)

The socket is a Wells-CTI #500-018-00, .050 c/c, 5-Lead Quad Flatpack Socket. This is also the socket used for the UT8Q512 and UT9Q512.

**Question 14**:)

The data sheets for the QCOTS SRAMs (i.e. UT7Q512, UT8Q512, and UT9Q512) note two solutions for total dose radiation performance. The differences behind these two solutions are listed below.

*Answer 14*:)

The two solutions refer to the intrinsic total dose performance of the SRAM die and additional radiation performance provided by the patented Aeroflex UTMC shielded package. Solution #1 is gained through the intrinsic radiation hardness of the SRAM die without the necessity of shielding. Solution #2, radiation performance of up to 300 krads, is orbit dependent, but gained through the use shielding by an alloy of Copper and Tungsten.

**Question 15**:)

What does the use of shielding offer the designer and how does it enhance the radiation performance of the integrated circuit?

*Answer 15*:)

Shielded package technology improves the life cycle of spaceborne integrated circuits (ICs) by shielding them from the damaging effects of space radiation. A shielded package extends the on-orbit lifetime of ICs by a factor of three to five times in low earth orbits (LEO) and from eight to ten times in geosynchronous orbits (GEO). The Aeroflex UTMC shielded package offers reduced weight over other shielding technologies and was awarded a U.S. Patent in September 2000.

**Question 16**:)

Whatis Aeroflex UTMC;s planfor higher bit density SRAM?

*Answer 16*:)

We will be stacking and evaluating an 8M QCOTS SRAM.

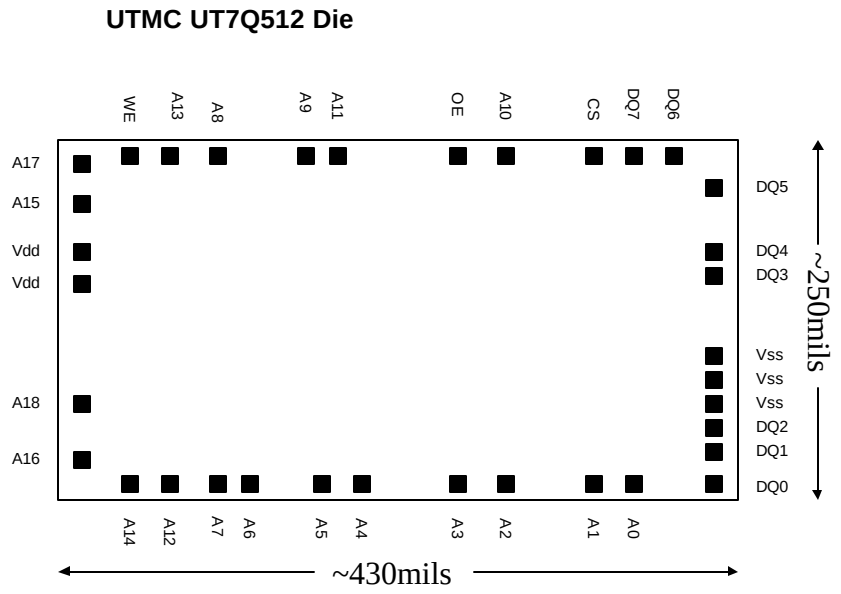


**Figure 1.** UT7Q512 Die Dimensions and Approximate X-Y Coordinates

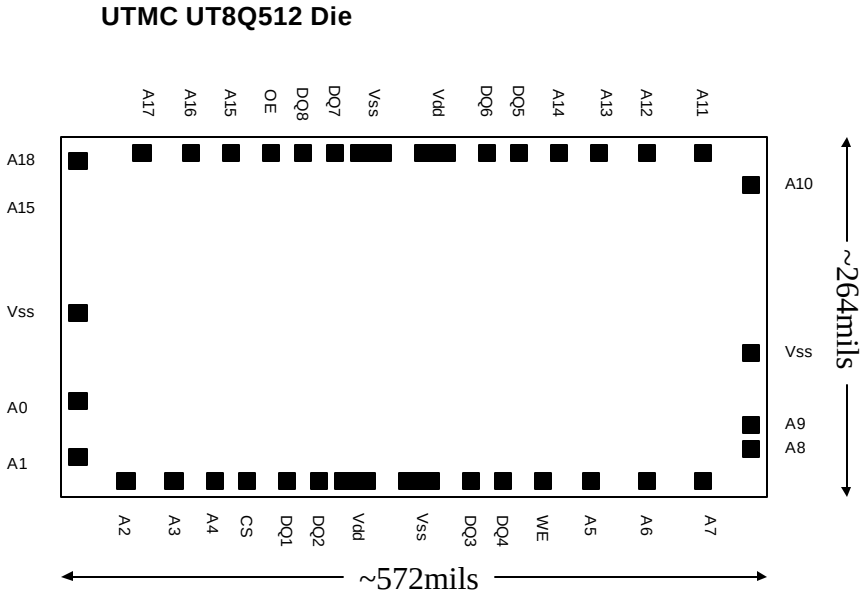


**Figure 2.** UT8Q512 and UT9Q512 Die Dimensions and Approximate X-Y Coordinates