Design Information Fact Sheet

UT8ER512K32 Monolithic 16M RadHard SRAM

FEATURES

- 20ns read, 10ns write maximum access times
- Functionally compatible with traditional 512K x 32 SRAM devices
- CMOS compatible inputs and output levels, three-state bidirectional data bus
  - 3.3 volt I/O, 1.8 volt core
- Radiation performance
  - Total-dose: >100Krad(Si)
  - SEL Immune: 100MeV-cm^2/mg
  - SEU error rate = 6.01x10^{-16} errors bit/day assuming geosynchronous orbit, Adam's 90% worst environment, and 156KHz default scrub rate (=99.4% SRAM availability)
  - Neutron Fluence: 3.0E14n/cm^2
- Packaging options:
  - 68-lead ceramic quad flatpack (6.898 grams)
- Standard Microcircuit Drawing 5962-06261
  - QML compliant part

INTRODUCTION

The UT8ER512K32 is a high-performance CMOS static RAM organized as 524,288 words by 32 bits. Easy memory expansion is provided by active LOW and HIGH chip enables ($\overline{E1}$, E2), an active LOW output enable ($\overline{G}$), and three-state drivers. This device has a power-down feature that reduces power consumption by more than 90% when deselected**.**

Writing to the device is accomplished by driving chip enable one ($\overline{E1}$) input LOW, chip enable two (E2) HIGH and write enable ($\overline{W}$) input LOW. Data on the 32 I/O pins (DQ0 through DQ31) is then written into the location specified on the address pins (A0 through A18). Reading from the device is accomplished by taking chip enable one ($\overline{E1}$) and output enable ($\overline{G}$) LOW while forcing write enable ($\overline{W}$) and chip enable two (E2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The 32 input/output pins (DQ0 through DQ31) are placed in a high impedance state when the device is deselected ($\overline{E1}$ HIGH or E2 LOW), the outputs are disabled ($\overline{G}$ HIGH), or during a write operation ($\overline{E1}$ LOW, E2 HIGH and $\overline{W}$ LOW).

UT8ER512K32 Master or Slave Options

To reduce bit error rates caused by single event phenomenon in space, the UT8ER512K32 employs an embedded EDAC (error detection and correction) with code engine with auto scrubbing. When a double bit error occurs in a word, the UT8ER512K32 asserts an $\overline{MBE}$ output to the host.

The UT8ER512K32 is offered in two options: Master or Slave. The UT8ER512K32M (Master) is a full function device capable of autonomous EDAC scrubbing which can also be used to demand scrub cycles on the UT8ER512K32S (Slave) by connecting the SCRUB pins on each device. The UT8ER512K32S (Slave) only performs EDAC scrub cycles when its SCRUB pin is driven by an external controller. The scrub-on-demand feature allows multiple UT8ER512K32S (Slave) devices to be controlled by one UT8ER512K32M (Master) device. The $\overline{SCRUB}$ function is a no connect (NC) on the UT8ER512K32S (Slave), and is used by the UT8ER512K32M (Master) to generate wait states in the memory controller. The $\overline{BUSY}$ function is an output on the Master device while on the Slave device it is an input.

RadHard 16M Monolithic SRAM Design Examples

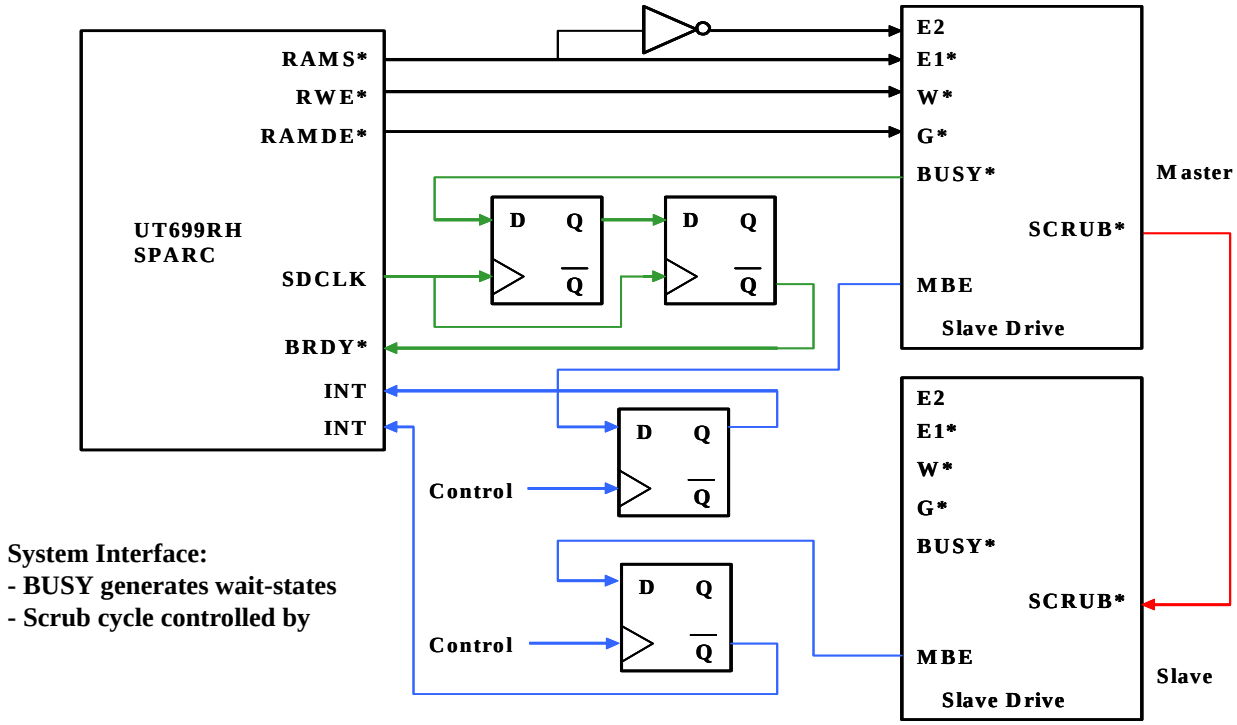


Figure 1. SPARC System Utilizing Master/Slave SRAMs with Auto-Scrub and Wait States

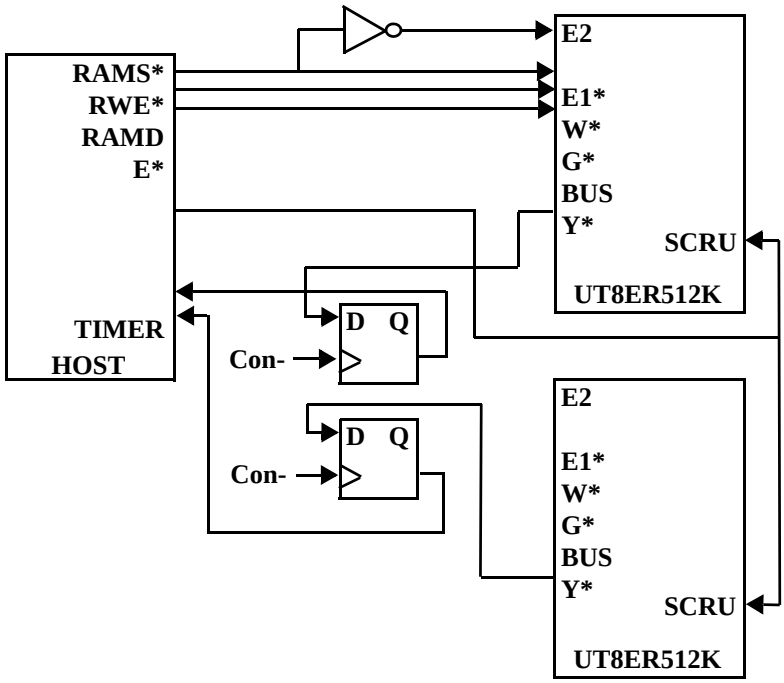


Figure 2. Slave Devices with Scrub-on-Command

16M SRAM Comparison to 4M SRAM

Design Factor	Industry Standard 4M SRAM	Aeroflex 16M SRAM
SEU Error Rate (errors / bit day)	**1.10^{-10}**	**$6x10^{-16}$ (4)**
Total Power Dissipation (16Mbit solution)	**1.5W (1,2)**	**0.6W (1,3)**
Total Land Area (16Mbit solution)	**4.8 sq-in (2)**	**3.0 sq-in (3)**

(1) Operating at 25 MHz and 125°C, V_{DD} = 3.3V
(2) Assumes four 4M memory devices
(3) Including 1.8V linear regulator
(4) Error rate assumes default 156KHz scrub frequency+

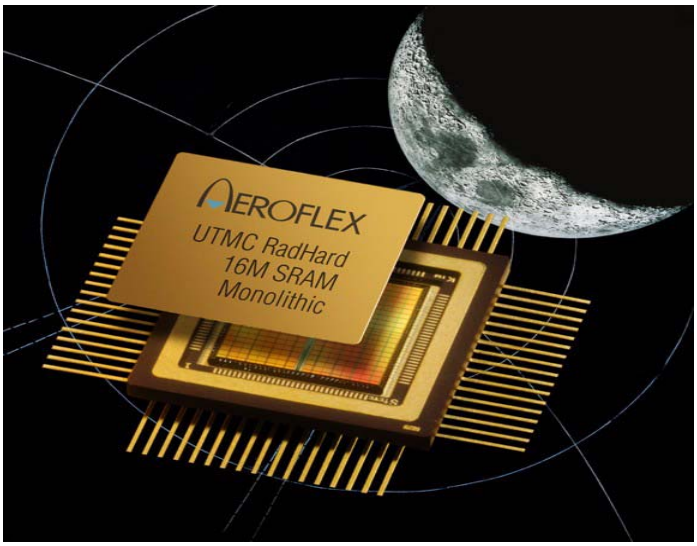
Value Proposition of RadHard 16M Monolithic SRAM

No need for external EDAC memory bits
Improved system speed
Reduces memory power consumption by 60% savings over individual components
Lower system cost (16M ASP is 2.5x a 4M)
40% area savings over 4M SRAMs using offchip EDAC device
Increased bits per square inch
Fast access time (50MHz operation)

Internet Resources:
Visit www.aeroflex.com/RadHardSRAM to download:

RadHard SRAM Data Sheets
Applications Notes
IBIS Models
Tutorial "How to Design with the RadHard 16M Monolithic SRAM"

Visit **www.aeroflex.com/RadHard** to see the latest
Aeroflex Colorado Springs' RadHard products for space applications!



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