Synchronous SRAM (SSRAM) READY Output Signal

Table 1: Cross Reference of Applicable Products

Product Name	Manufacturer Part Number	SMD Number	Device Type	Internal PIC* Number
64Mbit Synchronous SRAM	UT8SP2M32	5962-TBD	All	WN05
64Mbit Synchronous SRAM	UT8SF2M32	5962-TBD	All	WN06

* PIC: Aeroflex Product Information Code

1.0 Overview

This application note explains the purpose and function of the Synchronous SRAM (SSRAM) READY pin.

2.0 READY pin Description

The READY pin of the SSRAM device is an output pin which indicates when the device is ready for normal operations (HIGH). The READY pin indicates the completion of a manual or power on reset activity. The READY also notifies users when the device requires an idle cycle due to access conflicts between the user and background housekeeping task.

2.1 Technical Background

To achieve the SEE performance and data integrity demands of the space community, the Aeroflex SSRAM devices (Table 1) include autonomous internal error detection and error correction (EDAC) and fault detection. The EDAC and fault detection controllers perform internal housekeeping activities in the background during normal device operation. Conflicts between housekeeping and user access *may* cause the device READY output pin to de-assert (LOW), indicating the device requires an idle cycle to complete the housekeeping task. This application note explains why the READY pin de-asserts and how to operate the device to avoid a READY de-assertion and achieve maximum throughput.

2.1.0 *Memory Architecture and READY Function*

The Aeroflex SSRAM architecture consists of 128 memory banks. Executing housekeeping activities at regular intervals assures data integrity. Predominately these activities occur in memory banks not being accessed by the user. A conflict between the user and internal housekeeping occurs when both attempt to access the same memory bank. User's access is given priority by utilizing proprietary collision avoidance techniques. Internal housekeeping continues attempting to gain access to the bank with each subsequent clock cycle until successful (e.g. user exits bank), or the current internal housekeeping sequence ends. When a conflict remains at the end of a housekeeping sequence, the device allots an additional 64 clock cycles for the housekeeping bank access. If the user's bank access continues throughout the additional 64 clock cycles, the READY flag de-asserts. Once the READY flag de-asserts, the user should either change the bank address A(6:0) or provide an idle state within the next 16 clock cycles (reference Figure. 1 for READY de-assertion flow-chart). The housekeeping state machine waits indefinitely for the user to release the bank and will not continue with scheduled housekeeping sequences. For this reason, allowing READY to de-assert beyond 16 clock cycles will compromise data integrity.

3.0 How to Avoid READY De-Assertion

Users can avoid READY de-assertion due to memory bank conflicts with the internal device housekeeping by providing an idle cycle (deselecting any CS# input) once every 64 clock cycles, or changing the bank addressing (A6 - A0) at least once during every 64 clock cycles. Addressing the Aeroflex SSRAM in a sequential manner automatically causes the bank addresses to switch with each access.

4.0 Summary and Conclusion

The Aeroflex SSRAM employes internal EDAC and fault detection to achieve data integrity. The SSRAM EDAC and fault detection housekeeping activities are autonomous and invisible to the user. Conflicts between internal and user accesses occur when both attempt to access the same memory bank. If a conflict is present at the end of a housekeeping sequence, an additional 64 clock cycles occur before the READY flag de-asserts. Once the READY flag de-asserts, the user must resolve the conflict within the next 16 clock cycles or risk compromising data integrity. System designers can avoid READY de-assertions by providing an idle cycle once every 64 clock cycles, or switching bank addressing at least once every 64 clock cycles. If the user's system adheres to these recommendations, 100% of the memory bandwidth is available.
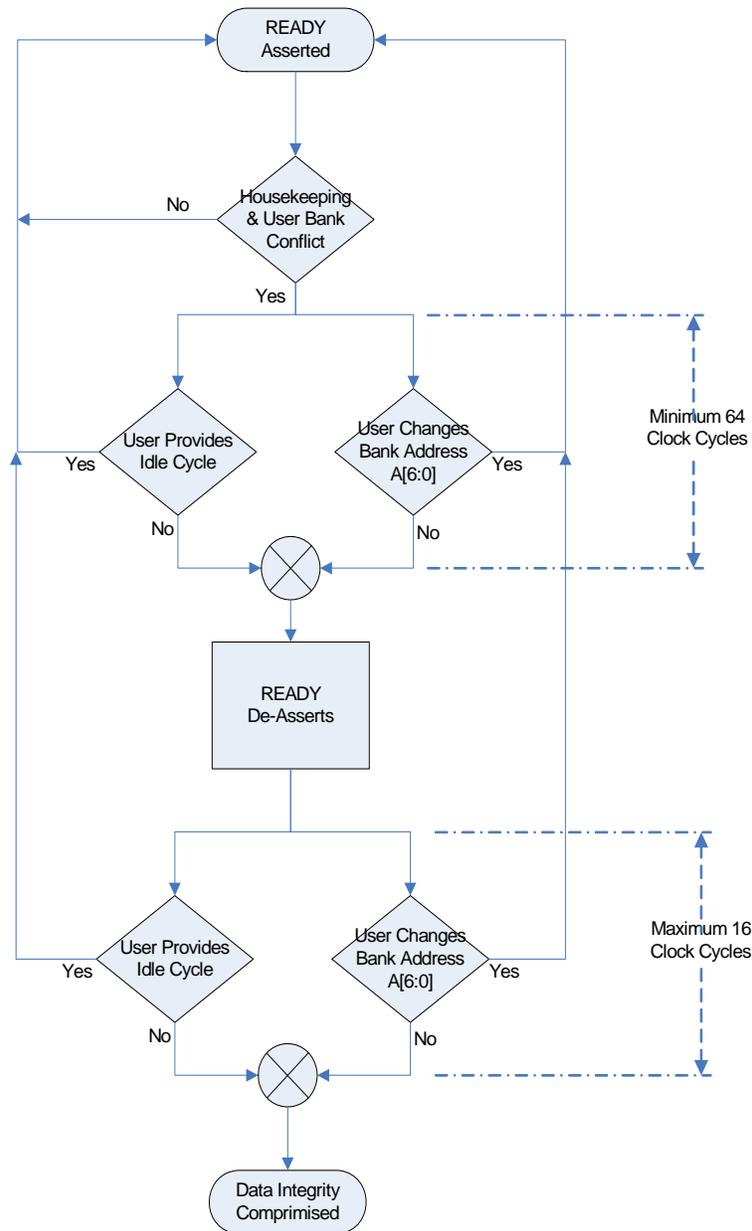

Figure. 1 READY Flowchart