

Next-Generation Embedded Processors Empower Satellite Telemetry and Command Systems



By Dave Stevenson, Systems Group Manager
Aeroflex Colorado Springs

Future satellite applications will place a greater demand on telemetry and control systems for increased intelligence and performance. One method is an embedded processor card that can be used to implement a standard telemetry and control satellite system.

Among the challenges facing satellite manufacturers today are mechanical reliability, reduced power consumption, shrinking monetary budgets and increased demands for on-satellite data processing. Among radiation-hardened electronics, fault-tolerant processors play a key role. Identifying a set of solutions – from mechanical chassis to digital electronics – that fits within a given set of specifications is a problem facing satellite design and integrators. Modern technology is meeting the challenges of high-density space applications via radiation performance,

power, mechanical weight and form factor, standardized software development tools, and next-generation System-on-Chip (SoC) designs.

A Brief History of Satellite Evolution

In the early 1990s, NASA began outlining plans and initiating directives for a new, smaller spacecraft technology through smaller, faster, cheaper satellites. NASA recognized that smaller systems have some distinct advantages over large, costly spacecraft. A small spacecraft is pound-for-pound less expensive to produce and more tolerant of schedule and funding changes than a larger, more costly spacecraft. Small spacecraft are also less dependent on space-shuttle-sized launch vehicles to achieve orbit.

One key factor driving NASA's smaller, cheaper, faster mantra was that the organization needed to launch more

satellites and experiments using fewer program dollars. In the spirit of NASA's 1992 small satellite initiatives, space component manufacturers today strive to minimize risk, size, cost, and power, while pushing for the maximum performance allowable for a space-borne, high-reliability device.

Commercial Influences on Space Electronics Evolution

Many new technological advancements can be attributed to forces in the commercial and space markets. The commercial cellular phone market developed the SoC device as a solution to provide smaller, more power-efficient single IC devices that incorporated a mix of functions common to the telecommunications industry. The impact SoC technology has had in the cellular phone market is readily known by anyone that owned a five pound brick-sized cellular phone in the early 1990's and

Table 1: Radiation & Power Requirements

Device Type	Total Ionizing Dose (TID)	Single Event Induced Latch-up (SEL)	Single Event Induced Effects (SEU)	Weight	Performance/Power
Commercial SOC	Poor TID induced device high leakage current failure	Poor SEL induced high-current device failure	Poor performance causing processor corruption of memory & instructions	Excellent 2-grams low weight, plastic package	Excellent typically 15mW/MHz
Space SOC	Designed to meet at least 100 krads	Requires immunity to >100MeV @ 125 Degrees Centigrade	Requires design mitigation techniques to eliminate susceptibility	Good 18-grams most requirements dictate ceramic sealed packages	Excellent performance of space devices achieve slightly less power/MHz
Space Board (level product)	Designed to meet at least 100 krads	All board components used must have immunity to >100MeV @ 125 Degrees Centigrade	Design implements mitigation techniques to eliminate susceptibility	Poor/ greater than 1500 grams	Poor/ 100mW/MHz more components require additional power

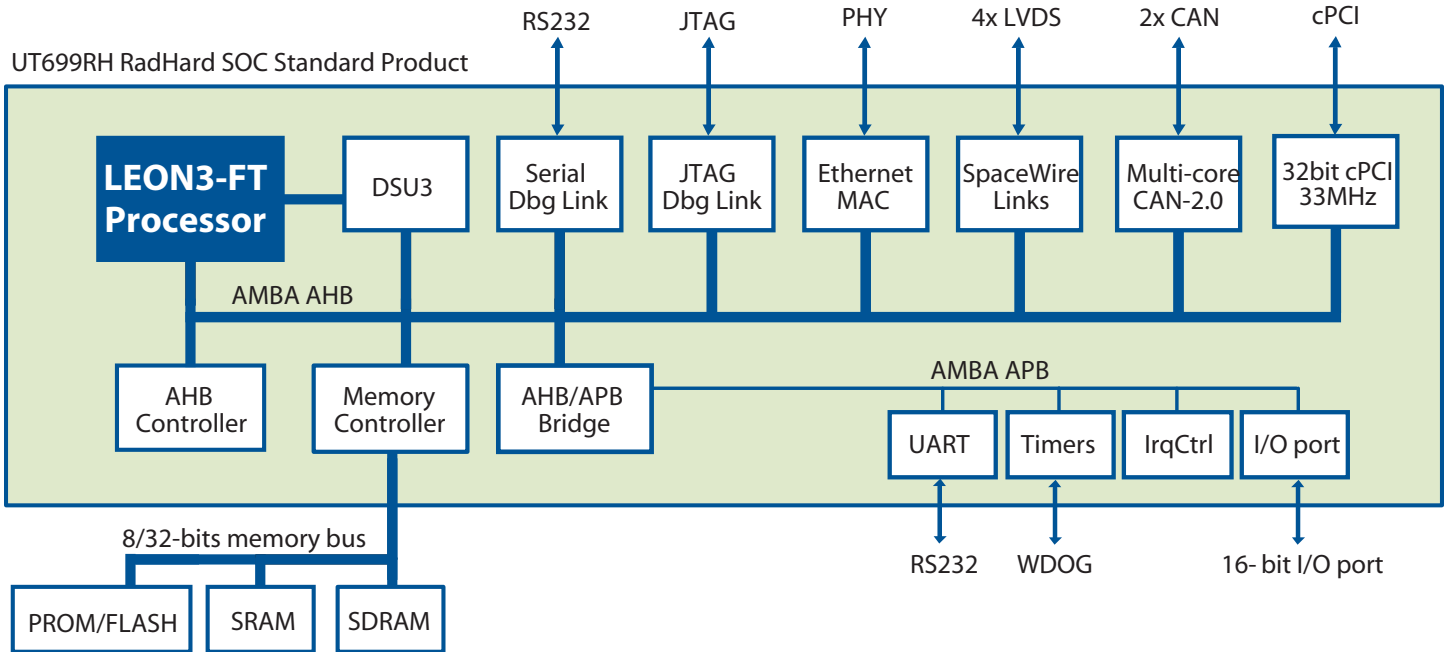


Figure 1: SOC Block Diagram Overview

now totes around one of the sleek, credit-card-sized phones offered today.

Space instrument and control system developers experimenting with SoC architectures are faced with additional challenges not seen in the commercial market segment. Although the SoC technology is readily available with many configurations that a satellite developer can theoretically use directly, using commercial technology in a space environment is not feasible because of the radiation exposure that occurs outside the protection of the earth's atmosphere. Table 1 outlines a collection of decision factors satellite designers must consider during space-borne component development.

Compilation of a Satellite Soc Device

SoC devices typically contain a processor, a set of support functions such as timers and interrupt controllers, as well as interface functions for external bus operations. Figure 1 illustrates an SoC device that incorporates common satellite bus interfaces, a memory controller, a fault-tolerant 32-bit SPARC and associated Debug Support Unit (DSU) integrated with an industry standard Advanced Microprocessor Bus Architecture (AMBA) bus.

Radiation Performance in Space

As stated earlier, one critical point to consider when selecting a component for use in a space environment is its radiation performance. The requirement to survive a multiyear space mission necessitates the use of radiation-hardened electronics in most satellite and space vehicles. The heart of any satellite control system is a radiation-hard processor designed with fault-tolerance as a goal, not an afterthought.

When selecting a component that is to be used in a radiation environment, always check the data sheet for assurances that the component will not have adverse operating effects when exposed to heavy ions or total

dose particles creating a system latch-up (high-current condition), or performance degradation during the satellite's operating life. A fault-tolerant processor will also reliably operate through harsh radiation conditions without generating illegal instruction cycles or corrupting program memory. The processor should be designed for operation in the space environment and should include the functionality to detect and correct Single Event Effects (SEEs) in all on-chip RAM memories (Table 2).

Minimizing power consumption

In addition to the criteria listed in Table 2, the space-borne SoC should implement a sleep mode halting the pipeline and

Table 2: SOC System SEE Criteria		
SOC Element	Single Event Effects	Single Event Latch-up
Internal Memory	Capability to detect and correct SEE errors	Capability to operate through >100MeV @ 125 Degrees Centigrade
Processor Instruction Execution	Designed with fault-tolerance creating total immunity to SEE	Capability to operate through >100MeV @ 125 Degrees Centigrade
Internal Registers	Capability to detect and correct SEE errors	Capability to operate through >100MeV @ 125 Degrees Centigrade

caches until an interrupt occurs, as well as clock controls to disable individual clocks to unused peripheral functions; this is an efficient way to minimize power consumption when the application is idle and should be accomplished without additional tool-specific software support.

The benefits achieved when using an SoC architecture include lower power consumption, higher performance, and higher reliability compared to a board-level solution. In addition to increased hardware efficiency, the modularity of the SoC architecture creates a natural platform for modular software development. These SoC technology advantages are readily apparent by studying a simple example application. Figure 2 illustrates a generic box-level Telemetry and Command (T&C) unit and a corresponding SoC solution that incorporates all the box-level functions into a single integrated circuit.

The T&C black box comprises four individual boards integrated through a backplane and weighing approximately 7 pounds or 3,200 grams. Each board in the

	Weight	Power
Black Box	3200 Grams	9 Watts
SOC	18 Grams	3 Watts
Net Savings	3182 Grams	6 Watts

T&C performs independent transactions to gather telemetry and command an attitude control system through a variety of bus types. The total power budget for the T&C box is approximately 9 W (Table 3). Note that most of the black box power is consumed through the interboard communications and not the spacecraft links. In contrast, the SoC device performs the same system transactions with less power and weight, approximately 3 W at 100 MHz and 18 grams respectively.

A key to weight control

Another factor linked to the production of a reliable smaller, cheaper satellite is the mechanical weight and form factor.

Compressing the area and mechanical features of a box-level component into a single device will not only dramatically reduce the weight, but increases overall reliability. To demonstrate, mechanical reliability includes assessment of mechanical dynamic loads within the electronic box; the calculation of these loads includes the Printed Wiring Boards (PWBs), the box backplane assembly, and each mechanical connection that connects one board to another. Therefore, a reliability assessment for the example box includes at least six mechanical failure points between two boards as illustrated in Figure 3. Combining all the functions from both boards into a single SoC integrated

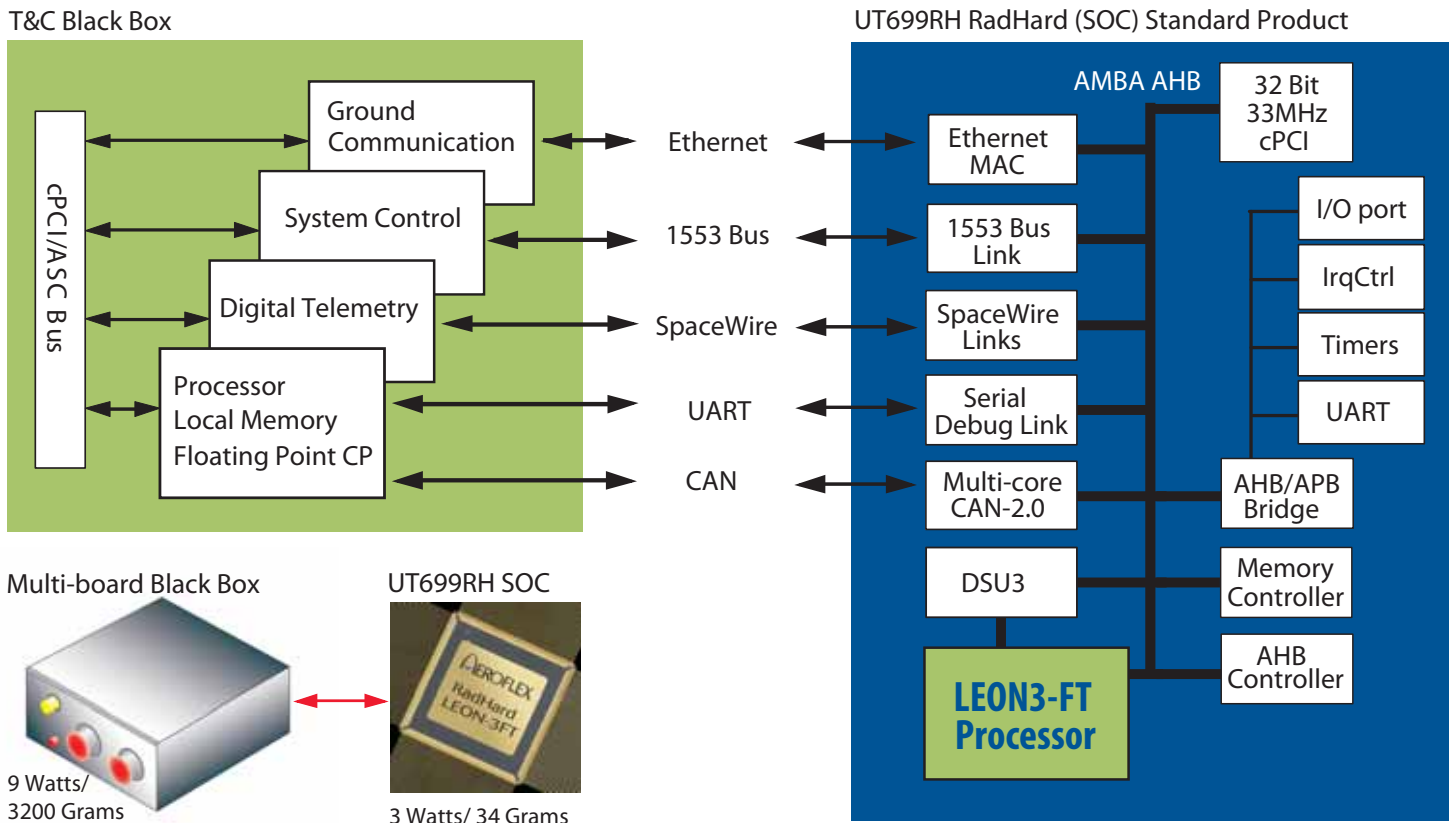


Figure 2: System Equivalency

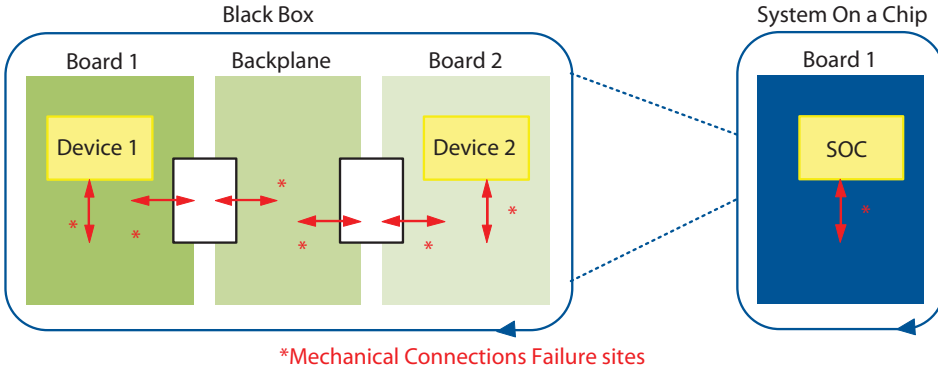


Figure 3: Mechanical Failure Site Comparison

circuit significantly reduces the board and backplane mechanical failure sites from six to one failure point because the entire system now resides on a single board.

SoC software development support

A final decision factor with regard to selecting an SoC is processor support by third-party software development tools. Since numerous functions (processor and

peripherals) reside in a single SoC circuit, the developer has limited visibility of the device’s interworkings. Magnifying this issue is the fact that qualified satellite flight equipment is scrutinized through rigorous testing to validate the hardware and software elements of the system. Table 4 highlights a few of the issues a designer should consider before settling on an SOC solution.

A System-on-Chip device with a set of features that seamlessly integrates to third-party tool suite as listed in Table 4 will provide enough functionality to satisfy most flight-qualified satellite software requirements while enabling SoC test and evaluation with common ground test equipment.

Next-gen processor-based applications in space

In conclusion, since much time and energy is expended to test and qualify a satellite system, software support and debug capability must be a key decision factor when choosing SoC components. The next generation of processor-based applications for space will be centered around SoC solutions that support the hardware, software, and radiation capabilities described. An embedded processor coupled to an SoC device architecture will be a key player in future satellite systems, accelerating development cycles through modularity while improving performance and reliability.

Table 4: Software Support Criteria

Software	Hardware Debug
Support by third-party, industry standard development tool suites and compilers	Support for non-intrusive hardware debug through a standard interface port (Ethernet, RS232, etc.)
Real-time operating support by third-party, industry standard development tool suites and compilers	Watch-point set support for address and/or instruction execution
Software development environment support by a variety of platforms and operating systems	Breakpoint set based on address and/or instruction execution allowing trace and single-stepping of the processor execution
	Full access to all SOC memory and register elements



Dave Stevenson, P.E.
Systems Group Manager
Aeroflex Colorado Springs

4350 Centennial Blvd.
 Colorado Springs, CO 80907
 (800) 645-8862
 dave.stevenson@aeroflex.com
 www.aeroflex.com/RadHard