RadHard-By-Design integrated circuit suppliers: A success story

By Anthony Jordan

The telecommunications and defense industries demand ever increasing functionality in space-based equipment such as satellites, probes, and spacecraft. Also, as high altitude and low earth orbit aircraft become increasingly reliant on sophisticated electronics, the demand for radiation-hardened and radiation-tolerant ICs has never been greater. To bring modern, leading-edge ICs to market quicker than ever requires the technical skills and capabilities of RadHard-By-Design (RHBD) suppliers.

Radiation-Hardened Requirement	Strategic Military System	Commercial Space System
Dose Rate Survivability	>1x10^{11}rad(Si)/s	N/A
Dose Rate Upset	>5x10^{9}rad(Si)/s	N/A
Survive accumulated total dose (TID)	>5x10^{5}krad(Si)	100k to 300krad(Si)
Charge particle strike induced upset	<1x10^{-7} errors per bit-day	<1x10^{-7} errors per bit-day
Immune to charge particle strike Induced latch-up	>100MeV-cm^2/mg	>80MeV-cm^2/mg
Neutron Fluence (neutrons per centimeter squared)	1x10^{14}	N/A

Table 1

In the late 1990s, a group of fabless integrated circuit suppliers wanted to serve the satellite marketplace. Success in the marketplace hinged on the ability of these companies to radiation-harden ICs by design using the intrinsic hardness of leading-edge wafer fabrication process technology. Suppliers embracing the new business model adopted the title of RadHard-By-Design (RHBD) or RadHard Fab-Independent integrated circuit suppliers. To the industry, RHBD promised space-ready leading-edge products, ending a decades-old trend of relying on ICs that were one or more generations behind the best-in-class devices.

The industry lined up both pro and con as to whether the RHBD companies would succeed. In question: Could RHBD techniques mitigate the effects of space rate ionizing dose (Total Ionizing Dose or TID), large rates of ionizing dose (Dose Rate Upset or Survival, DRU and DRS), neutron strikes, and charged particle strikes (commonly referred to as *Single Event Effects* or SEE). Table 1 describes the radiation-hardness requirements of strategic military and commercial space systems. The goal of RHBD suppliers is to achieve the radiation-hardened requirements shown in Table 1 via a combination of circuit design techniques and physical design techniques. In some cases, minimally invasive process modifications are used to improve the integrated circuit's radiation performance.

Key in the fab-independent RHBD business model was access to leading-edge commercial wafer processing technology. Emerging wafer foundries supplied RHBD companies with access to leading-edge commercial wafer processing technology without large capital and labor expense investments. RHBD companies were able move from 0.6um CMOS to 130nm with some having an eye on state-of-the-art 90 nm technologies, outpacing the stereotypical radiation-hardened integrated device manufacturers (for example, radiation-hardened suppliers with their own wafer foundries).

By definition, fab-independent and RHBD integrated circuit suppliers subcontract wafer manufacturing to commercial wafer foundries. Wafers are then probed, background, sawn, packaged, environmentally screened, and electrically tested prior to shipment to customers. With the exception of wafer foundry, all other aspects of technology and product development are performed by the RHBD supplier, as shown in Figure 1.

Total Ionizing Dose mitigation

As the RHBD companies raced to smaller processing nodes, a few interesting things happened. TID performance improved in most processes, and Single Event Effects became a dominant problem. TID immunity improved on average from less than 100k rads(Si) to greater than 100k rads(Si) for process technologies below 250 nm. Improved TID performance was the direct result of processes moving to thinner gate oxides from Localized Oxidation of Silicon (LOCOS) processes to Shallow Trench Isolation (STI) at the 0.25µ process node. The combination of shallow trench isolation processing and physical design rules that limit inter- and intratransistor leakage has been very effective; these techniques yield functional and parametric circuit designs with greater than 100k rad(Si) performance for dense designs. Figure 2 shows intradevice and interdevice leakage paths that form as a result of exposure to ionizing energy.

Single Event Effect mitigation

While the goal of achieving total ionizing dose levels for Geosynchronous Earth Orbit (GEO) missions has been helped by decreasing process geometries, gate oxide thicknesses and the use of STI other effects have become more problematic. The techniques to mitigate the effects of charge particle strikes, Single Event Effects, had to evolve due to smaller, more densely packed transistors: Single Event Latch-up (SEL), Single Event Upset (SEU), and Single Event Transients (SET).

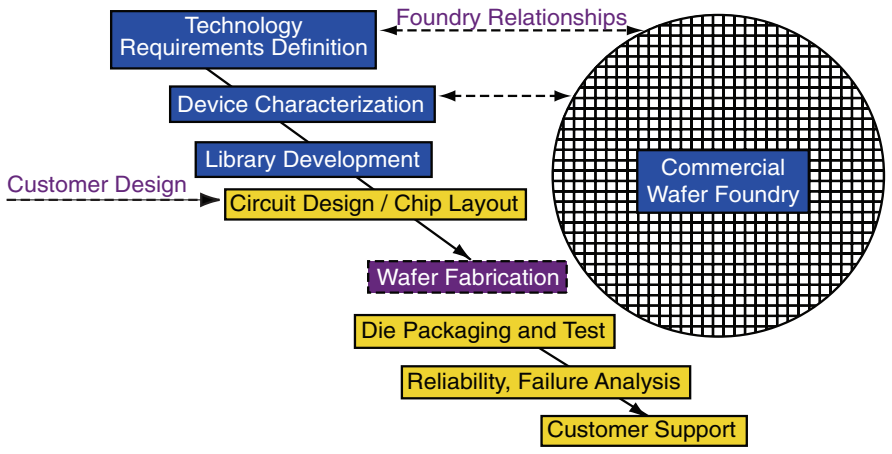

Figure 1

Decreased active area spacing has led to increased single event latch-up sensitivity. As a result, RHBD suppliers must absorb area penalties to mitigate these latch-ups that occur as a result of galactic cosmic ray and solar ions coming from the sun. First, the gain of parasitic bipolar transistors must be lowered ($ß_{NPN}ß_{PNP} << 1$) to avoid latch-up. Lowering parasitic transistor gain is accomplished by reducing transistor base width and collector efficiency. A bullet-proof solution requires guard rings to eliminate the four-layer SCR structure. Second, to reduce well and substrate resistance, extra ties increase overall circuit size.

After mitigating SEL, the RHBD suppliers must address SEU and SET as a result of charge particle strikes. Decreasing transistor size and parasitic capacitance has decreased the electrical charge (for example, critical charge Q_c) required to upset a storage element (flip-flop, latch, memory cell). This, in turn, has led to more Single Event Effects errors. Successful techniques to mitigate Single Event Effects include Triple Mode Redundancy (TMR), dual redundancy, spatial time clocking, and error detection and correction. TMR involves the two-out-of-three voting of outputs to determine the proper logic state of sequential circuits. TMR circuits pay area, power, and speed penalties due to the increased flip-flop count and combinatorial logic layers (voting circuit). RHBD suppliers using TMR techniques typically use minimum area flip-flops, latches, and combinatorial circuits to offset the speed, area, and power penalties associated with the TMR circuit.

An alternative is to use redundancy in the storage element to mitigate particle strikes. In the case of redundancy, sensitive critical nodes within flip-flops and latches are made redundant and spaced apart to prevent a single ion from upsetting both critical nodes. The drive strengths of transistors controlling critical nodes are also sized to reduce the effect of charged particle strikes. Redundant circuits have a smaller area penalty than TMR circuits but are larger than conventional commercial flip-flops or latches and burn more power than minimum configuration commercial flip-flops and latches. Redundant flip-flops and latches also pay a speed and power penalty due to the increased cell complexity and larger transistors on size controlling sensitive nodes.

Another proven technique in the mitigation of charge-particle-induced upset and transients is the use of multiple phases of the clock coupled to a majority vote circuit. Using small differences in clock phase to create "N" samples of the data presented to "N" sequential circuits and then voting the "N" outcomes effectively filters out both upsets and transient upsets in the sequential circuit. Temporal clocking circuits are also larger, slower, and burn more power than minimum size commercial flip-flops and latches. Note that the temporal clocking technique addresses both upset and transient effects, whereas TMR and redundant latch techniques do not. Last, but not least, is Error Detection And Correction or EDAC. Typically used in memory circuits, EDAC uses check bits to reconstruct or restore a stored data word in the event of an upset or error.

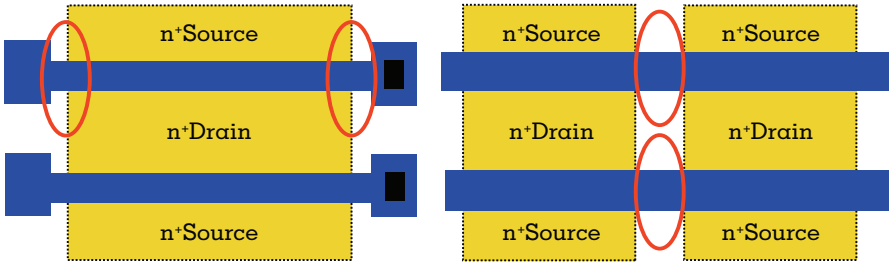

Figure 2

Dose rate effects

When ionization occurs over a short period of time (for example, 20 to 50 ns), large photocurrents occur, resulting in upset and latch-up. As a result of these photocurrents, circuits may exhibit logic-state upset due to power supply droop sometimes called *rail collapse*. Photocurrent can also trigger destructive latch-up or metal burnout. These phenomena are referred to as *Dose Rate Upset* and *Dose Rate Latch-Up* respectively. RHBD suppliers mitigate the effects of large photocurrents by using special spatial layout rules and techniques to limit parasitic NPN and PNP gains.

Emerging EDA issues

While the RHBD companies escaped the multi-hundred-million-dollar semiconductor equipment and process development bill, they must absorb the cost of Electronic Design Automation (EDA) tools required to develop deep and ultra-deep submicron integrated circuits. Behavioral language tools in conjunction with verified IP blocks (DSP, memory, memory controllers, processors, and so forth) have swollen gate counts to well over a million gates. With the gate count increase, the cost of design verification, functionality, design margin evaluation, and physical design verification has risen to hundreds of thousands of dollars. The budget to staff a complete design team may approach or even exceed several million dollars. New tools to evaluate signal integrity, leakage current, power distribution and IR analysis, and low power synthesis, further increased the cost of a deep submicron EDA tools set (for example, the latest release of a foundry reference flow includes foundry-validated techniques for power optimization, power analysis, Design For Manufacturing (DFM), area reduction, chip and package integration, and flip chip area I/O design).

Originally planned for use in commercial and civilian satellites, RHBD integrated circuits are now used in not only commercial and civilian satellites but military satellites as well. Keys to penetrating the various space market segments were not only performance, function, and radiation hardness but also reliability. Mission life requirements have increased from 7 to 10 years to more than 15 years with goals of 20 years on the horizon. With increasing mission and operating life, reliability remains a key attribute of space-grade integrated circuits. To address these reliability requirements, RadHard suppliers combined military-specified design methodologies and analysis with robust physical cell libraries and mature, well-controlled, high-volume wafer foundries.

The future of RHBD

RadHard-By-Design is a viable design approach for supplying space application integrated circuits. Several suppliers have adopted this business model during the past 5 to 10 years to build strong competitive companies. They continue to bring advanced integrated circuits to the marketplace, meeting the requirements of all segments of the satellite marketplace (civilian, military, and commercial space). As they move forward, these companies will have to mitigate new radiation effects as process geometries shrink and to understand how new materials will react after exposure to ionizing radiation and charge particle strikes. The future for these companies looks promising.

Anthony Jordan *is currently director-standard products. He has been at Aeroflex Colorado Springs for 16 years and brings 22 years of semiconductor experience to the company. Anthony has held various standard product marketing and applications engineering positions with Aeroflex (formerly UTMC). He received his BSEE degree from Bradley University and MSEE from Rochester Institute of Technology. To learn more, contact Anthony at:*

Aeroflex Colorado Springs
4350 Centennial Blvd.
Colorado Springs, CO 80907
Tel: 719-594-8252
E-mail: Jordan@Aeroflex.com
Website: www.aeroflex.com/radhard