

# Aeroflex Colorado Springs Errata

---

**Date:** March 24, 2008

**Part Number:** UT8ER512K32 Monolithic 16M RadHard SRAM

**Silicon Revision:** Revision B Prototypes

**Affected Date Codes:** All Revision B Prototypes

## Data Sheet Specification for UT8ER512K32M and UT8ER512K32S

### RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS
$V_{DD1}$	DC supply voltage (Core)	1.7 to 1.9V
$V_{DD2}$	DC supply voltage (I/O)	3.0 to 3.6V
$V_{IN}$	DC input voltage	0V to $V_{DD2}$

## Errata Specification for UT8ER512K32M and UT8ER512K32S

### RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS
$V_{DD1}$	DC supply voltage (Core)	<b>1.8 to 2.0V</b>
$V_{DD2}$	DC supply voltage (I/O)	3.0 to 3.6V
$V_{IN}$	DC input voltage	0V to $V_{DD2}$

# Aeroflex Colorado Springs Errata

## Data Sheet Specification for UT8ER512K32M (not applicable for UT8ER512K32S)

Table 4: EDAC Programming Configuration Table			
ADDR BIT	PARAMETER	VALUE	FUNCTION
A (0 - 3)	Scrub Rate <sup>1</sup>	0-15	As Scrub Rate changes from 0 - 15, then the interval between Scrub cycles will change as follows: 0 = 20 MHz      6 = 312 kHz      11 = 9.76 kHz 1 = 10 MHz      7 = 156 kHz      12 = 4.88 kHz 2 = 5 MHz      8 = 78 kHz      13 = 2.44 kHz 3 = 2.5 MHz      9 = 39 kHz      14 = 1.22 kHz <sup>4</sup> 4 = 1.25 MHz      10 = 19.5 kHz      15 = .61 kHz <sup>4</sup> 5 = 625 kHz
A (4 - 7)	$\overline{\text{BUSY}}$ to $\overline{\text{SCRUB}}$ <sup>2</sup>	0-15	If $\overline{\text{BUSY}}$ changes from 0 - 15, then the interval $t_{\text{BLSL}}$ between $\overline{\text{SCRUB}}$ and $\overline{\text{BUSY}}$ will change as follows: 0 = 0 ns      6 = 300 ns      11 = 550 ns 1 = 50 ns      7 = 350 ns      12 = 600 ns 2 = 100 ns      8 = 400 ns      13 = 650 ns 3 = 150 ns      9 = 450 ns      14 = 700 ns 4 = 200 ns      10 = 500 ns      15 = 750 ns 5 = 250 ns
A (8)	Bypass EDAC Bit <sup>3</sup>	0, 1	If 0, then normal EDAC operation will occur. If 1, then EDAC will be bypassed.
A (9)	Read / Write Control Register	0, 1	0 = A0 to A8 will be written to the control register 1 = Control register will be asserted to the data bus

**Notes:**

1. Default Scrub Rate is 156KHz.
2. The default for  $t_{\text{BLSL}}$  is 500 ns.
3. The default state for A8 is 0.
4. Below testing capability.

# Aeroflex Colorado Springs Errata

## Errata Specification for UT8ER512K32M (not applicable for UT8ER512K32S)

Table 4: EDAC Programming Configuration Table			
ADDR BIT	PARAMETER	VALUE	FUNCTION
A (0 - 3)	Scrub Rate <sup>1</sup>	0-15	As Scrub Rate changes from 0 - 15, then the interval between Scrub cycles will change as follows: 0 = 20 MHz      6 = 312 kHz      11 = 9.76 kHz 1 = 10 MHz      7 = 156 kHz      12 = 4.88 kHz 2 = 5 MHz      8 = 78 kHz      13 = 2.44 kHz 3 = 2.5 MHz      9 = 39 kHz      14 = 1.22 kHz <sup>4</sup> 4 = 1.25 MHz      10 = 19.5 kHz      15 = .61 kHz <sup>4</sup> 5 = 625 kHz
A (4 - 7)	$\overline{\text{BUSY}}$ to $\overline{\text{SCRUB}}$ <sup>2</sup>	0-15	If $\overline{\text{BUSY}}$ changes from 0 - 15, then the interval $t_{\text{BLSL}}$ between $\overline{\text{SCRUB}}$ and $\overline{\text{BUSY}}$ will change as follows: 0 = 0 ns      6 = 300 ns      11 = 550 ns 1 = 50 ns      7 = 350 ns      12 = 600 ns 2 = 100 ns      8 = 400 ns      13 = 650 ns 3 = 150 ns      9 = 450 ns      14 = 700 ns 4 = 200 ns      10 = 500 ns      15 = 750 ns 5 = 250 ns
A (8)	Bypass EDAC Bit <sup>3</sup>	0	If 0, then normal EDAC operation will occur.
A (9)	Read / Write Control Register	0	0 = A0 to A8 will be written to the control register

**Notes:**

1. Default Scrub Rate is 156KHz.
2. The default for  $t_{\text{BLSL}}$  is 500 ns.
3. The default state for A8 is 0.
4. Below testing capability.