

Customer Owned Tooling Services (COTS)

Fact Sheet

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www.aeroflex.com/RadHardASIC



Overview:

Aeroflex Colorado Springs's Customer Owned Tooling Services (COTS) design flow allows the designer to take advantage of an ASIC process that can optimize performance, power, die size, and functionality. By using COTS, designers need only one vendor for ASIC design processing, design fabrication, package assembly and test.

AEROFLEX CUSTOMER OWNED TOOLING SERVICES (COTS) DESIGN FLOW:

The designer:

- Completes the design using their own design tools with the target foundry's design rules, transistor models, etc.*
- Submits the design database in a GDS II format
- Has the option to submit stimulus/response results in a tabular "print on change" format

Aeroflex:

- Provides layout design rules for the target foundry to augment foundry's baseline
- Provides spice models (Level 28 in HSpice or BSIM 3 v 3) for target process technology for process variations (i.e. CRH modules)
- Integrates frame and test structures
- Verifies GDSII against foundry DRC, ERC, LVS run sets
- Completes pattern generation for design manufacturing
- Has the silicon built in the target wafer fab
- Ship wafers direct to customer after wafer process parametrics verified

Options:

- Electrically probes the wafers for functionality using customer provided stimulus/response results
- Packages prototype units
- Electrically tests package units for functionality using customer provided stimulus/response results
- Provides QML Q/V production assembly and screening as required

* - requires NDA or CDA from target foundry for the desired process technology

BENEFITS OF USING AEROFLEX'S COTS:

Custom design allows optimization and flexibility to meet the system requirements.

• Design Functions

Aeroflex offers special functions such as RAM, ROM, and a variety of megacells, standard cells, and datapath cells for custom designs. These functions can be supplied by Aeroflex, the customer, or third party sources.

• Design Performance

The performance of the design can be optimized to meet the customer's speed, density and power requirements.

• Die size/Pad Placement and Quantity

The die size can be minimized to reduce die cost.

I/O pad placement and pad quantity is optimized for each design.

• Design Flexibility

The customer design team is able to use any system or chip design process optimized for the design i.e., VHDL, Mentor, Cadence.

Aeroflex Colorado Springs - Datasheet Definition

Advanced Datasheet - Product In Development

Preliminary Datasheet - Shipping Prototype

Datasheet - Shipping QML & Reduced Hi-Rel

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