Standard Products

UT8R1M39 40Megabit SRAM MCM
UT8R2M39 80Megabit SRAM MCM
UT8R4M39 160Megabit SRAM MCM

Data Sheet

December 2015

The most important thing we build is trust

FEATURES

- 20ns Read, 10ns Write maximum access times available
- Functionally compatible with traditional 1M, 2M, or 4M x 39 SRAM devices
- CMOS compatible input and output levels, three-state bidirectional data bus
  - I/O Voltages 2.3V to 3.6V, 1.7V to 2.0V core
- Available densities:
  - UT8R1M39: 40, 894, 464 bits
  - UT8R2M39: 81, 788, 928 bits
  - UT8R4M39: 163, 577, 856 bits
- Operational Environment:
  - Total-dose: 100 krad(Si)
  - SEL Immune: ≤110 MeV-cm^2/mg
  - SEU error rate = 7.3x10^{-7} errors/bit-day assuming geosynchronous orbit, Adam's 90% worst environment.
- Packaging options:
  - 132-lead side-brazed dual cavity ceramic quad flatpack
- Standard Microelectronics Drawing:
  - UT8R1M39: 5962-10205
    - QML Q, Q+ and V compliant
  - UT8R2M39: 5962-10206
    - QML Q, Q+, and Vcompliant
  - UT8R4M39: 5962-10207
    - QML Q and Q+ compliant part

INTRODUCTION

The UT8R1M39, UT8R2M39, and UT8R4M39 are high performance CMOS static RAM multichip modules (MCMs) organized as two, four or eight individual 524,288 words x 39 bits dice respectively. Easy memory expansion is provided by active LOW chip enables ($\overline{En}$), an active LOW output enable ($\overline{G}$), and three-state drivers. This device has a power-down feature that reduces power consumption by more than 90% when deselected**.**

Writing to the device is accomplished by driving one of the chip enable ($\overline{En}$) inputs LOW and the write enable ($\overline{W}$) input LOW. Data on the 39 I/O pins (DQ0 through DQ38) is then written into the location specified on the address pins (A0 through A18). Reading from the device is accomplished by driving one of the chip enables ($\overline{En}$) and output enable ($\overline{G}$) LOW while driving write enable ($\overline{W}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins. **Note:** Only one $\overline{En}$ pin may be active at any time.

The 39 input/output pins (DQ0 through DQ38) are placed in a high impedance state when the device is deselected ($\overline{En}$ HIGH), the outputs are disabled ($\overline{G}$ HIGH), or during a write operation ($\overline{En}$ LOW, $\overline{W}$ LOW).

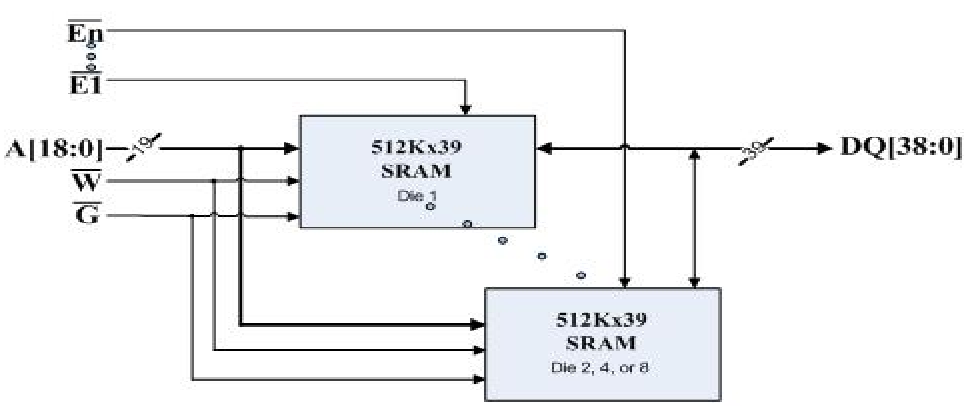
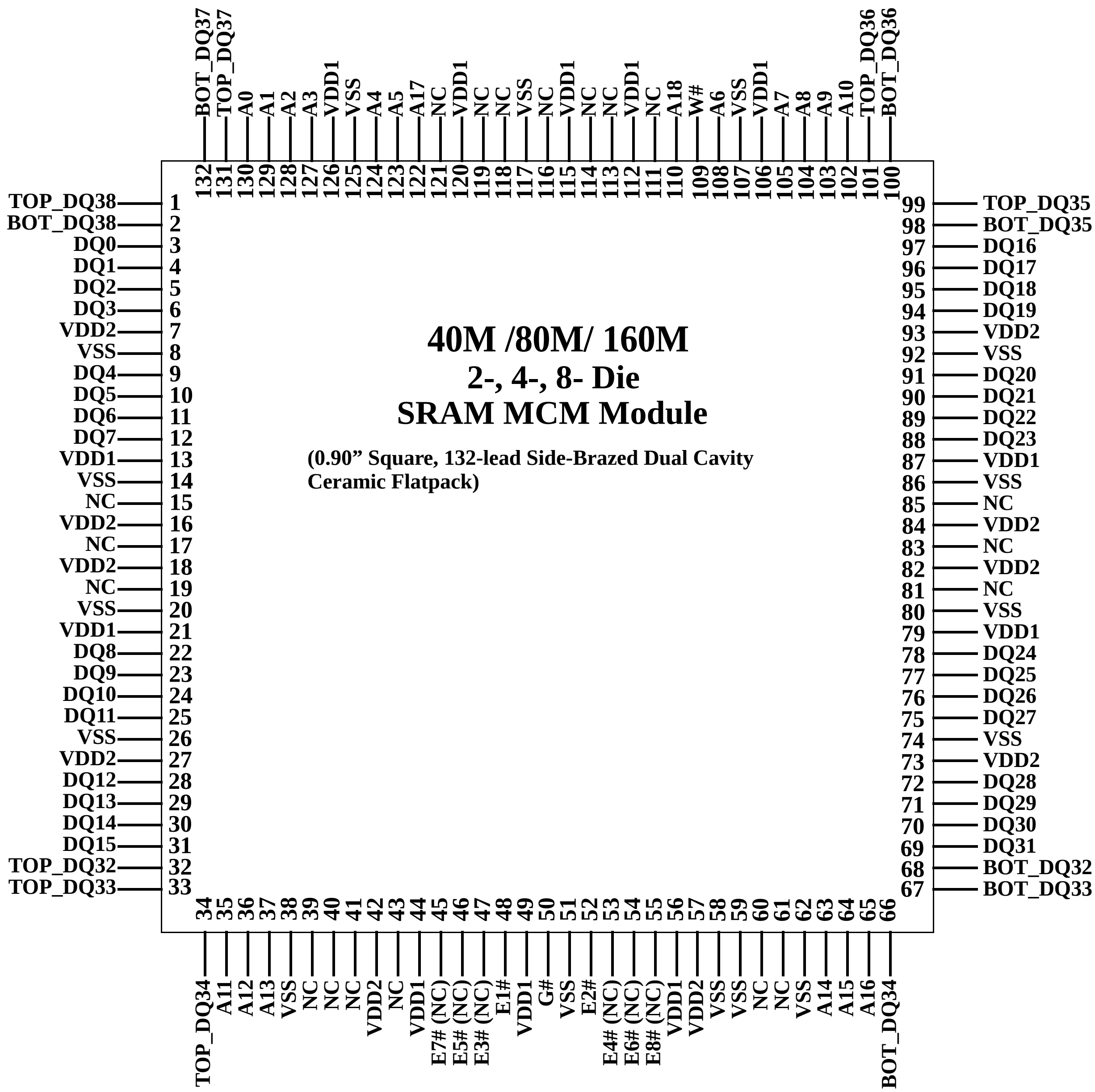


Figure 1. Block Diagram



Notes:
1. NC=Pins are not connected on die.
2. (NC) = Depending on product version, the pin may be either an enable signal as named or NC.
3. Each TOP and BOT signal for DQ38 through DQ32 must be externally connected by user.

Figure 2. Pin Diagram

Table 1. Pin Description

Pin	Type	Description
A(18:0)	I	Address Input
DQ(31:0)	BI	Data Input/Output
En#*	I	Enable (Active Low)
W#	I	Write Enable (Active Low)
G#	I	Output Enable (Active Low)
VDD1	P	Power (1.8V nominal)
VDD2	P	Power (3.3V nominal)
VSS	P	Ground

Notes:
* n represents any number of individual MCM (multichip module) die enables. May be 1-8 depending on device option.

Table 2. Device Option: Signal and Pin Description

Package Pin Number	UT8R1M39 Signal Name	UT8R2M39 Signal Name	UT8R4M39 Signal Name	Device Pin Description
1	TOP_DQ38	TOP_DQ38	TOP_DQ38	Data I/O[1]
2	BOT_DQ38	BOT_DQ38	BOT_DQ38	Data I/O[1]
3	DQ0	DQ0	DQ0	Data I/O
4	DQ1	DQ1	DQ1	Data I/O
5	DQ2	DQ2	DQ2	Data I/O
6	DQ3	DQ3	DQ3	Data I/O
7	VDD2	VDD2	VDD2	PWR
8	VSS	VSS	VSS	PWR
9	DQ4	DQ4	DQ4	Data I/O
10	DQ5	DQ5	DQ5	Data I/O
11	DQ6	DQ6	DQ6	Data I/O
12	DQ7	DQ7	DQ7	Data I/O
13	VDD1	VDD1	VDD1	PWR
14	VSS	VSS	VSS	PWR
15	NC	NC	NC	NC
16	VDD2	VDD2	VDD2	PWR
17	NC	NC	NC	NC
18	VDD2	VDD2	VDD2	PWR
19	NC	NC	NC	NC
20	VSS	VSS	VSS	PWR
21	VDD1	VDD1	VDD1	PWR
22	DQ8	DQ8	DQ8	Data I/O
23	DQ9	DQ9	DQ9	Data I/O
24	DQ10	DQ10	DQ10	Data I/O
25	DQ11	DQ11	DQ11	Data I/O
26	VSS	VSS	VSS	PWR
27	VDD2	VDD2	VDD2	PWR
28	DQ12	DQ12	DQ12	Data I/O
29	DQ13	DQ13	DQ13	Data I/O

Table 2. Device Option: Signal and Pin Description

Package Pin Number	UT8R1M39 Signal Name	UT8R2M39 Signal Name	UT8R4M39 Signal Name	Device Pin Description
30	DQ14	DQ14	DQ14	Data I/O
31	DQ15	DQ15	DQ15	Data I/O
32	TOP_DQ32	TOP_DQ32	TOP_DQ32	Data I/O[1]
33	TOP_DQ33	TOP_DQ33	TOP_DQ33	Data I/O[1]
34	TOP_DQ34	TOP_DQ34	TOP_DQ34	Data I/O[1]
35	A11	A11	A11	ADDRESS INPUT
36	A12	A12	A12	ADDRESS INPUT
37	A13	A13	A13	ADDRESS INPUT
38	VSS	VSS	VSS	PWR
39	NC	NC	NC	NC
40	NC	NC	NC	NC
41	NC	NC	NC	NC
42	VDD2	VDD2	VDD2	PWR
43	NC	NC	Nc	NC
44	VDD1	VDD1	VDD1	PWR
45	NC	NC	E7#	CONTROL INPUT[2]
46	NC	NC	E5#	CONTROL INPUT[2]
47	NC	E3#	E3#	CONTROL INPUT[2]
48	E1#	E1#	E1#	CONTROL INPUT
49	VDD1	VDD1	VDD1	PWR
50	G#	G#	G#	CONTROL INPUT
51	VSS	VSS	VSS	PWR
52	E2#	E2#	E2#	CONTROL INPUT
53	NC	E4#	E4#	CONTROL INPUT[2]
54	NC	NC	E6#	CONTROL INPUT[2]
55	NC	NC	E8#	CONTROL INPUT[2]
56	VDD1	VDD1	VDD1	PWR
57	VDD2	VDD2	VDD2	PWR
58	VSS	VSS	VSS	PWR
59	VSS	VSS	VSS	PWR
60	NC	NC	NC	NC

Table 2. Device Option: Signal and Pin Description

Package Pin Number	UT8R1M39 Signal Name	UT8R2M39 Signal Name	UT8R4M39 Signal Name	Device Pin Description
61	NC	NC	NC	NC
62	VSS	VSS	VSS	PWR
63	A14	A14	A14	ADDRESS INPUT
64	A15	A15	A15	ADDRESS INPUT
65	A16	A16	A16	ADDRESS INPUT
66	BOT_DQ34	BOT_DQ34	BOT_DQ34	Data I/O[1]
67	BOT_DQ33	BOT_DQ33	BOT_DQ33	Data I/O[1]
68	BOT_DQ32	BOT_DQ32	BOT_DQ32	Data I/O[1]
69	DQ31	DQ31	DQ31	Data I/O
70	DQ30	DQ30	DQ30	Data I/O
71	DQ29	DQ29	DQ29	Data I/O
72	DQ28	DQ28	DQ28	Data I/O
73	VDD2	VDD2	VDD2	PWR[1]
74	VSS	VSS	VSS	PWR
75	DQ27	DQ27	DQ27	Data I/O
76	DQ26	DQ26	DQ26	Data I/O
77	DQ25	DQ25	DQ25	Data I/O
78	DQ24	DQ24	DQ24	Data I/O
79	VDD1	VDD1	VDD1	PWR
80	VSS	VSS	VSS	PWR
81	NC	NC	NC	NC
82	VDD2	VDD2	VDD2	PWR
83	NC	NC	NC	NC
84	VDD2	VDD2	VDD2	PWR
85	NC	NC	NC	NC
86	VSS	VSS	VSS	PWR
87	VDD1	VDD1	VDD1	PWR
88	DQ23	DQ23	DQ23	Data I/O
89	DQ22	DQ22	DQ22	Data I/O
90	DQ21	DQ21	DQ21	Data I/O

Table 2. Device Option: Signal and Pin Description

Package Pin Number	UT8R1M39 Signal Name	UT8R2M39 Signal Name	UT8R4M39 Signal Name	Device Pin Description
91	DQ20	DQ20	DQ20	Data I/O
92	VSS	VSS	VSS	PWR
93	VDD2	VDD2	VDD2	PWR
94	DQ19	DQ19	DQ19	Data I/O
95	DQ18	DQ18	DQ18	Data I/O
96	DQ17	DQ17	DQ17	Data I/O
97	DQ16	DQ16	DQ16	Data I/O
98	BOT_DQ35	BOT_DQ35	BOT_DQ35	Data I/O[1]
99	TOP_DQ35	TOP_DQ35	TOP_DQ35	Data I/O[1]
100	BOT_DQ36	BOT_DQ36	BOT_DQ36	Data I/O[1]
101	TOP_DQ36	TOP_DQ36	TOP_DQ36	Data I/O[1]
102	A10	A10	A10	ADDRESS INPUT
103	A9	A9	A9	ADDRESS INPUT
104	A8	A8	A8	ADDRESS INPUT
105	A7	A7	A7	ADDRESS INPUT
106	VDD1	VDD1	VDD1	PWR
107	VSS	VSS	VSS	PWR
108	A6	A6	A6	ADDRESS INPUT
109	W#	W#	W#	CONTROL INPUT
110	A18	A18	A18	ADDRESS INPUT
111	NC	NC	NC	NC
112	VDD1	VDD1	VDD1	PWR
113	NC	NC	NC	NC
114	NC	NC	NC	NC
115	VDD1	VDD1	VDD1	PWR
116	NC	NC	NC	NC
117	VSS	VSS	VSS	PWR
118	NC	NC	NC	NC
119	NC	NC	NC	NC
120	VDD1	VDD1	VDD1	PWR
121	NC	NC	NC	NC

Table 2. Device Option: Signal and Pin Description

Package Pin Number	UT8R1M39 Signal Name	UT8R2M39 Signal Name	UT8R4M39 Signal Name	Device Pin Description
122	A17	A17	A17	ADDRESS INPUT
123	A5	A5	A5	ADDRESS INPUT
124	A4	A4	A4	ADDRESS INPUT
125	VSS	VSS	VSS	PWR
126	VDD1	VDD1	VDD1	PWR
127	A3	A3	A3	ADDRESS INPUT
128	A2	A2	A2	ADDRESS INPUT
129	A1	A1	A1	ADDRESS INPUT
130	A0	A0	A0	ADDRESS INPUT
131	TOP_DQ37	TOP_DQ37	TOP_DQ37	Data I/O[1]
132	BOT_DQ37	BOT_DQ37	BOT_DQ37	Data I/O[1]

Notes:
NC pins are not connected on the die.
1. Each TOP and BOT signal pin for DQ38 through DQ32 must be externally connected together by user.
2. Control input when declared as En#, otherwise pin is NC.

DEVICE OPERATION

The SRAMs have control inputs called Chip Enable ($\overline{En}$), Write Enable ($\overline{W}$), and Output Enable ($\overline{G}$); 19 address inputs, A(18:0); and 39 bidirectional data lines, DQ(38:0). The $\overline{En}$ (chip enable) controls selection between active and standby modes. Asserting $\overline{En}$ enables the device, causes I_{DD} to rise to its active value, and decodes the 19 address inputs. Only one chip enable may be active at anytime. $\overline{W}$ controls read and write operations. During a read cycle, $\overline{G}$ must be asserted to enable the outputs.

Table 2. SRAM Device Control Operation Truth Table

$\overline{G}$	$\overline{W}$	$\overline{En}$	I/O Mode	Mode
X	X	H	DQ(38:0) 3-State	Standby
L	H	L	DQ(38:0) Data Out	Word Read
H	H	L	DQ(38:0) All 3-State	Word Read[2]
X	L	L	DQ(38:0) Data In	Word Write

Notes:
1. "X" is defined as a "don't care" condition.
2. Device active; outputs disabled.

READ CYCLE

A combination of $\overline{W}$ greater than V_{IH} (min) with a single $\overline{En}$ and $\overline{G}$ less than V_{IL} (max) defines a read cycle. Read access time is measured from the latter of device enable, output enable, or valid address to valid data output.

SRAM Read Cycle 1, the Address Access in Figure 3a, is initiated by a change in address inputs after a single $\overline{En}$ is asserted, $\overline{G}$ is asserted, $\overline{W}$ is deasserted and are all stable. Valid data appears on data outputs DQ(38:0) after the specified t_{AVQV} is satisfied. Outputs remain active throughout the entire cycle. As long as device enable and output enable are active, the minimum time between valid address changes is specified by the read cycle time (t_{AVAV1}).

SRAM Read Cycle 2, the Chip Enable-controlled Access in Figure 3b, is initiated by a single $\overline{En}$ going active while $\overline{G}$ remains asserted, $\overline{W}$ remains deasserted, and the addresses remain stable for the entire cycle. After the specified t_{ETQV} is satisfied, the 39-bit word addressed by A(18:0) is accessed and appears at the data outputs DQ(38:0).

SRAM Read Cycle 3, the Output Enable-controlled Access in Figure 3c, is initiated by $\overline{G}$ going active while a single $\overline{En}$ is asserted, $\overline{W}$ is deasserted, and the addresses are stable. Read access time is t_{GLQV} unless t_{AVQV} or t_{ETQV} (reference Figure 3b) have not been satisfied.

WRITE CYCLE

A combination of $\overline{W}$ and a single $\overline{En}$ less than V_{IL}(max) defines a write cycle. The state of $\overline{G}$ is a "don't care" for a write cycle. The outputs are placed in the high-impedance state when either $\overline{G}$ is greater than V_{IH}(min), or when $\overline{W}$ is less than V_{IL}(max).

Write Cycle 1, the Write Enable-controlled Access in Figure 4a, is defined by a write terminated by $\overline{W}$ going high, with a single $\overline{En}$ still active. The write pulse width is defined by t_{WLWH} when the write is initiated by $\overline{W}$, and by t_{ETWH} when the write is initiated by $\overline{En}$. To avoid bus contention t_{WLQZ} must be satisfied before data is applied to the 39 bidirectional pins DQ(38:0) unless the outputs have been previously placed in high impedance state by deasserting $\overline{G}$.

Write Cycle 2, the Chip Enable-controlled Access in Figure 4b, is defined by a write terminated by a single $\overline{En}$. The write pulse width is defined by t_{WLEF} when the write is initiated by $\overline{W}$, and by t_{ETEF} when the write is initiated by $\overline{En}$ going active. For the $\overline{W}$ initiated write, unless the outputs have been previously placed in the high-impedance state by $\overline{G}$, the user must wait t_{WLQZ} before applying data to the 39 bidirectional pins DQ(38:0) to avoid bus contention.

Table 3. Operational Environment[1]

Total Dose	100K	radsSi)
Heavy Ion Error Rate[2]	$7.3x10^{-7}$	Errors/Bit-Day

Notes:

1. The SRAM is immune to latchup to particles ≤110MeV-cm²/mg.
2. 90% worst case particle environment, Geosynchronous orbit, 100 mils of Aluminum.

SUPPLY SEQUENCING

No supply voltage sequencing is required between V_{DD1} and V_{DD2}.

POWER-UP REQUIREMENTS

During power-up of the SRAM devices, the power supply voltages will traverse through voltage ranges where the device is not guaranteed to operate before reaching final levels. Since some circuits on the device may operate at lower voltage levels than others, the device may power-up in an unknown state. To eliminate this with most power-up situations, the device employs an on-chip power-on-reset (POR) circuit. The POR, however, requires time to complete the operation. Therefore, it is recommended that all device activity be delayed by a minimum of 100ms, after both V_{DD1} and V_{DD2} supplies have reached their respective minimum operating voltages.

EXTERNAL CONNECTION REQUIREMENTS

Bidirectional data lines DQ38-DQ32 have both a TOP and BOT pinout. TOP and BOT for each data line must be externally connected together by user.

ABSOLUTE MAXIMUM RATINGS[1]

(Referenced to V_{SS})

SYMBOL	PARAMETER	LIMITS
V_{DD1}	DC supply voltage (Core)	-0.3 to 2.1V
V_{DD2}	DC supply voltage (I/O)	-0.3 to 3.8V
$V_{I/O}$	Voltage on any pin	-0.3 to 3.8V
T_{STG}	Storage temperature	-65 to +150°C
P_D[2] UT8R1M39 UT8R2M39 UT8R4M39	Maximum package power dissipation permitted @ Tc = +105°C	3.3W 2W 1.3W
T_J	Maximum junction temperature	+150°C
Θ_{JC}[3] UT8R1M39 UT8R2M39 UT8R4M39	Thermal resistance, junction-to-case[2]	6°C/W 10°C/W 15°C/W
I_I	DC input current	±10 mA

Notes:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2. Per MIL-STD-883, Method 1012, Section 3.4.1, $P_D = \frac{(125^{o}C - 105^{o}C)}{\Theta_{JC}}$
3. Θ_{JC} varies with density due to stacked die configuration.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS
V_{DD1}	DC supply voltage (Core)	1.7 to 2.0V
V_{DD2}	DC supply voltage (I/O)	2.3 to 3.6V
T_C	Case temperature range	-55°C to +105°C
V_{IN}	DC input voltage	0V to V_{DD2}

DC ELECTRICAL CHARACTERISTICS (Pre and Post-Radiation)*

(V_{DD1} = 1.7V to 2.0V, V_{DD2} = 2.3V to 3.6V; Unless otherwise noted, Tc is per the temperature range ordered)

SYMBOL	PARAMETER	CONDITION		MIN	MAX	UNIT
V_{IH}	High-level input voltage			2.2		V
V_{IL}	Low-level input voltage				0.8	V
V_{OL1}	Low-level output voltage	I_{OL} = 8mA, 3.0V≤V_{DD2} ≤ 3.6V			0.4	V
V_{OL2}	Low-level output voltage	I_{OL} = 6mA, 2.3V≤V_{DD2} ≤ 2.7V			0.2*V_{DD2}	
V_{OH1}	High-level output voltage	I_{OH} = -4mA, 3.0V≤V_{DD2} ≤ 3.6V		0.8*V_{DD2}		V
V_{OH2}	High-level output voltage	I_{OL} = -2mA, 2.3V≤V_{DD2} ≤ 2.7V		0.8*V_{DD2}		
I_{IN}	Input leakage current	V_{IN} = V_{DD2} and V_{SS}		-2	2	µA
I_{OZ}	Three-state output leakage current	V_O = V_{DD2} and V_{SS} V_{DD2} = V_{DD2} (max), $\overline{G}$ = V_{DD2} (max)		-2	2	µA
I_{OS}[2,3]	Short-circuit output current	V_{DD2} = V_{DD2} (max), V_O = V_{DD2} V_{DD2} = V_{DD2} (max), V_O = V_{SS}		-100	+100	mA
$I_{DD1}(OP_1)$[5]	V_{DD1} Supply current read operation @ 1MHz	Inputs: V_{IL} = V_{SS} + 0.2V, V_{IH} = V_{DD2} -0.2V, I_{OUT} = 0 V_{DD2} = V_{DD2} (max)	V_{DD1}= 2.0V		14	mA
			V_{DD1} = 1.9V		10	mA
$I_{DD1}(OP_2)$[5,6]	V_{DD1} Supply current read operation @ fmax	Inputs: V_{IL} = V_{SS} + 0.2V, V_{IH} = V_{DD2} -0.2V, I_{OUT} = 0 V_{DD2} = V_{DD2} (max)	V_{DD1} = 2.0V V_{DD1} = 1.9V UT8R4M39		230 215	mA mA
			V_{DD1} = 2.0V V_{DD1} = 1.9V UT8R1M39 UT8R2M39		225 210	mA mA
$I_{DD2}(OP_1)$[5]	V_{DD2} Supply current read operation @ 1MHz	Inputs : V_{IL} = V_{SS} + 0.2V, V_{IH} = V_{DD2} -0.2V, I_{OUT} = 0 V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max)			2	mA
$I_{DD2}(OP_2)$[5,6]	V_{DD2} Supply current read operation @ fmax	Inputs : V_{IL} = V_{SS} + 0.2V, V_{IH} = V_{DD2} -0.2V, I_{OUT} = 0 V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max)			5	mA

SYMBOL	PARAMETER	CONDITION		MIN	MAX	UNIT
$I_{DD1}(SB)^{4,7}$	Supply current standby @ 0Hz (per die)	CMOS inputs, I_{OUT} = 0 $\overline{En}$ = V_{DD2} -0.2 V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max)	-55°C and 25°C		15	mA
			105°C		35	mA
$I_{DD2}(SB)^{7}$	Supply current standby @ 0Hz (per die)	CMOS inputs, I_{OUT} = 0 $\overline{En}$ = V_{DD2} -0.2 V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max)			3	mA
$I_{DD1}(SB)^{4,6,7}$	Supply current standby A(16:0) @ fmax (per die)	CMOS inputs , I_{OUT} = 0 $\overline{En}$ = V_{DD2} - 0.2 V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max)	-55°C and 25°C		15	mA
			105°C		35	mA
$I_{DD2}(SB)^{6,7}$	Supply current standby A(16:0) @ fmax (per die)	CMOS inputs, I_{OUT} = 0 $\overline{En}$ = V_{DD2} - 0.2 V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max)			3	mA

CAPACITANCE

SYMBOL	PARAMETER	CONDITION	UT8R1M39		UT8R2M39		UT8R4M39		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
C_{IN}[1]	Input capacitance	f = 1MHz @ 0V		18		29		50	pF
C_{En}[1]	Input capacitance Device Enables	f = 1MHz @ 0V		10		10		10	pF
C_{IO}[1] DQ(31:0)	Bidirectional I/O capacitance	f = 1MHz @ 0V		15		27		50	pF
C_{IO}[1] TOP and BOT DQ(38:32)	Bidirectional I/O capacitance	f = 1MHz @ 0V		10		20		32	pF

Notes:

* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.
1. Measured only for initial qualification and after process or design changes that could affect this parameter.
2. Supplied as a design limit but not guaranteed nor tested.
3. Not more than one output may be shorted at a time for maximum duration of one second.
4. Post radiation limits are the 105°C temperature limit when specified.
5. Operating current limit does not include standby current.
6. fmax =50MHz.
7. V_{IH} = V_{DD2} (max), V_{IL} = 0V.

AC CHARACTERISTICS READ CYCLE (Pre and Post-Radiation)*

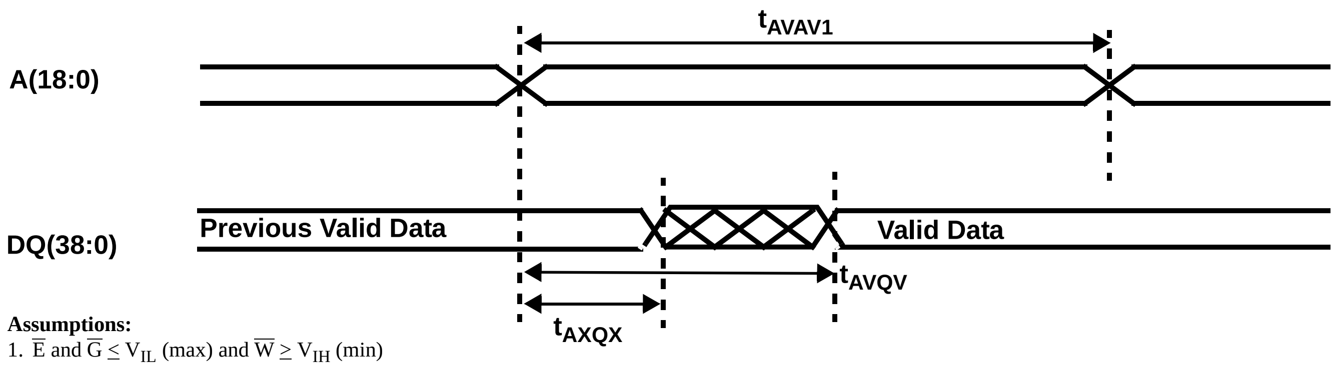
(V_{DD1} = 1.7V to 2.0V, V_{DD2} = 2.3V to 3.6V; Unless otherwise noted, Tc is per the temperature range ordered.)

SYMBOL	PARAMETER	UT8R1M39		UT8R2M39		UT8R4M39		UNIT	FIGURE
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{AVAV1}[1]	Read cycle time	20		22		25		ns	3a
t_{AVQV}	Address to data valid from address change		20		22		25	ns	3c
t_{AXQX}[2]	Output hold time	3		3		3		ns	3a
t_{GLQX}[1,2]	$\overline{G}$-controlled output enable time	2		2		2		ns	3c
t_{GLQV}	$\overline{G}$-controlled output data valid		8		8		10	ns	3c
t_{GHQZ}[2]	$\overline{G}$-controlled output three-state time	2	6	2	6	1	8	ns	3c
t_{ETQX}[2]	E-controlled output enable time	5		5		5		ns	3b
t_{ETQV}	E-controlled access time		20		22		25	ns	3b
t_{EFQZ}[2]	E-controlled output three-state time[2]	2	7	2	7	2	7	ns	3b

Notes:

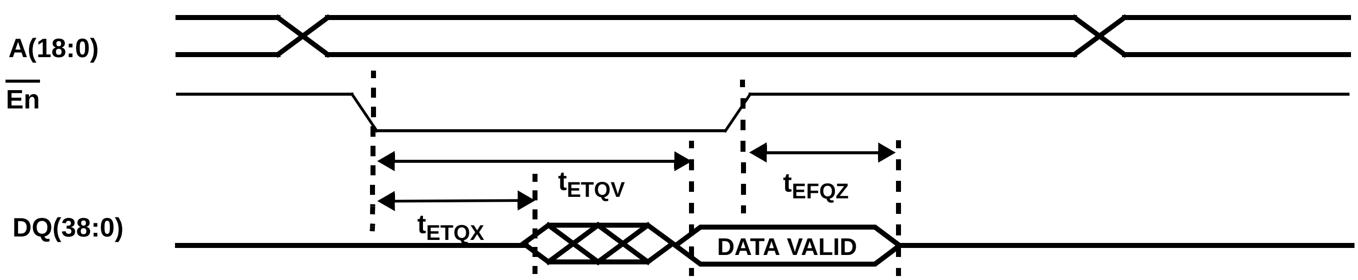
* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured

1. Guaranteed by characterization, but not tested.
2. Three-state is defined as a change from steady-state output voltage.



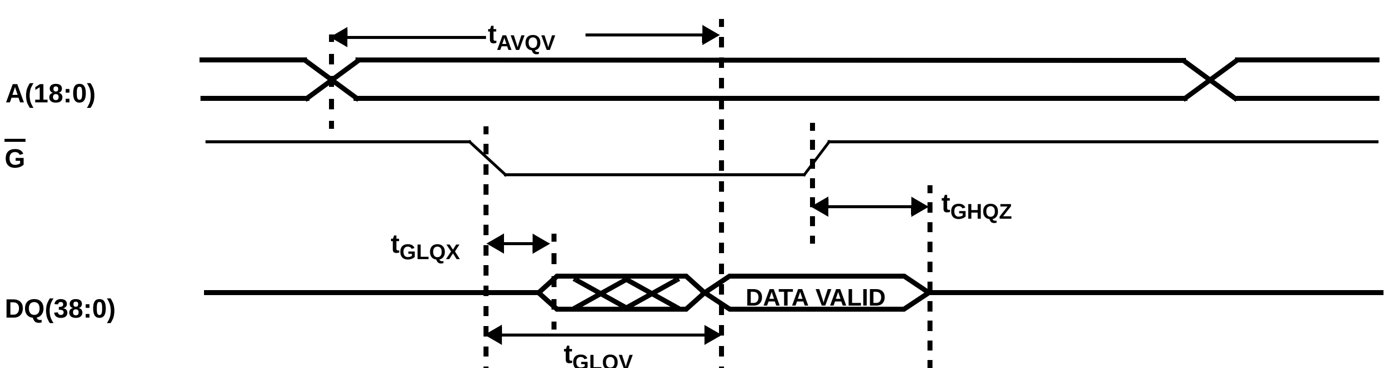
Assumptions:
1. $\overline{E}$ and $\overline{G} \leq V_{IL}$ (max) and $\overline{W} \geq V_{IH}$ (min)

Figure 3a. SRAM Read Cycle 1: Address Access



Assumptions:
1. $\overline{G} \leq V_{IL}$ (max) and $\overline{W} \geq V_{IH}$ (min)

Figure 3b. SRAM Read Cycle 2: Chip Enable-Controlled Access



Assumptions:
1. $\overline{E} \leq V_{IL}$ (max) and $\overline{W} \geq V_{IH}$ (min)

Figure 3c. SRAM Read Cycle 3: Output Enable Access

AC CHARACTERISTICS WRITE CYCLE (Pre and Post-Radiation)*

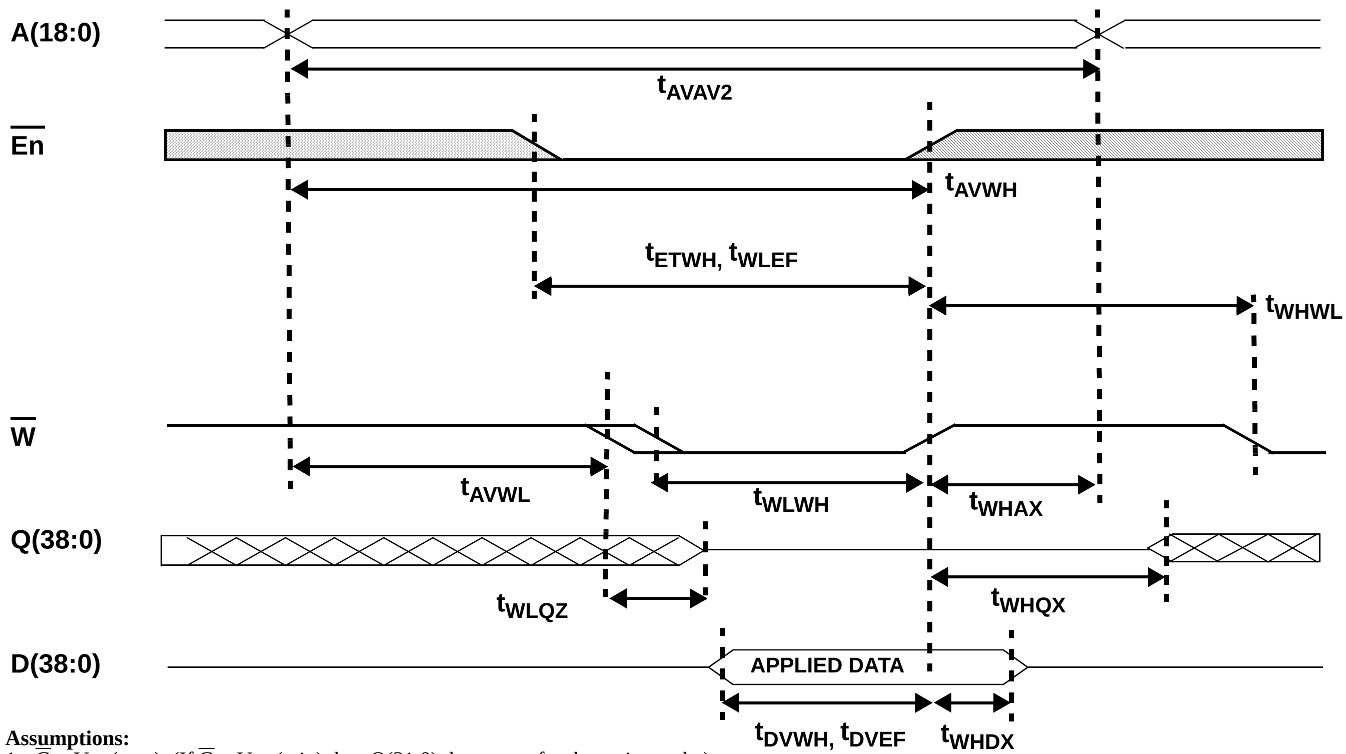
(V_{DD1} = 1.7V to 2.0V, V_{DD2} = 2.3V to 3.6V; Unless otherwise noted, Tc is per the temperature range ordered.)

SYMBOL	PARAMETER	UT8R1M39		UT8R2M39		UT8R4M39		UNIT	FIGURE
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{AVAV2}[1]	Write cycle time	10		10		10		ns	4a/4b
t_{ETWH}	Device enable to end of write	10		10		10		ns	4a
t_{AVET}	Address setup time for write ($\overline{En}$- controlled)	0		0		0		ns	4b
t_{AVWL}	Address setup time for write ($\overline{W}$ - controlled)	0		0		0		ns	4a
t_{WLWH}[1]	Write pulse width	8		8		8		ns	4a
t_{WHAX}	Address hold time for write ($\overline{W}$ - controlled)	0		0		0		ns	4a
t_{EFAX}	Address hold time for device enable ($\overline{En}$- controlled)	0		0		0		ns	4b
t_{WLQZ}[2]	$\overline{W}$ - controlled three-state time		7		7		9	ns	4a/4b
t_{WHQX}[2]	$\overline{W}$ - controlled output enable time	0		0		0		ns	4a
t_{ETEF}	Device enable pulse width ($\overline{En}$ - controlled)	10		10		10		ns	4b
t_{DVWH}	Data setup time	5		5		6		ns	4a
t_{WHDX}	Data hold time	0		0		0		ns	4a
t_{WLEF}[1]	Device enable controlled write pulse width	8		8		8		ns	4b
t_{DVEF}	Data setup time	5		5		6		ns	4a/4b
t_{EFDX}	Data hold time	0		0		0		ns	4b
t_{AVWH}	Address valid to end of write	10		10		10		ns	4a
t_{WHWL}[1]	Write disable time	2		2		3		ns	4a

Notes:

* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured

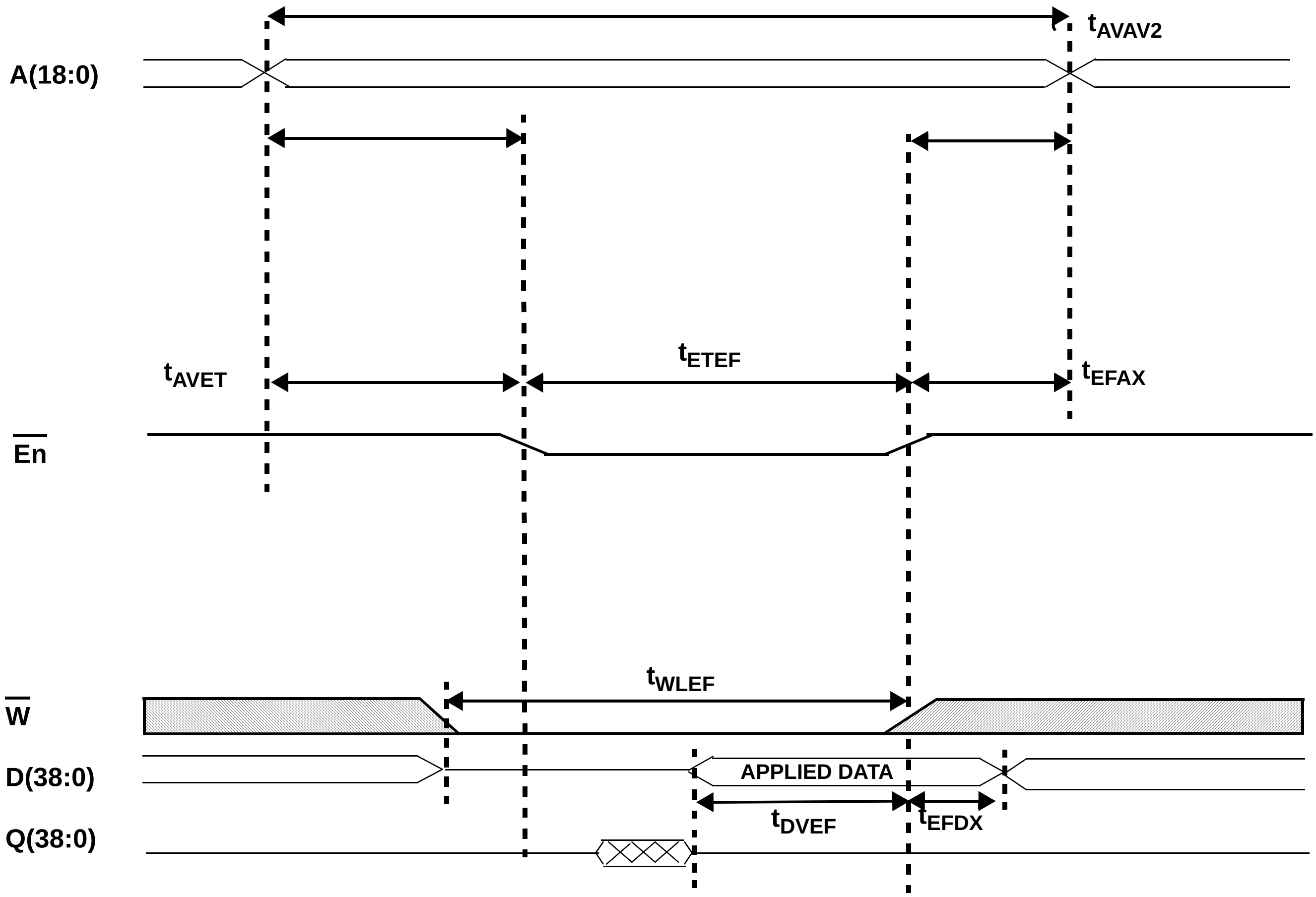
1. Tested with $\overline{G}$ high.
2. Three-state is defined as a change from steady-state output voltage.



Assumptions:

1. $\overline{G} \leq V_{IL}$ (max). (If $\overline{G} \geq V_{IH}$ (min) then Q(31:0) three-state for the entire cycle.)

Figure 4a. SRAM Write Cycle 1: $\overline{W}$ - Controlled Access



Assumptions & Notes:
1. $\overline{G} \leq V_{IL}$ (max). (If $\overline{G} \geq V_{IH}$ (min) then Q(31:0) three-state for the entire cycle.)

Figure 4b. SRAM Write Cycle 2: Enable - Controlled Access

DATA RETENTION CHARACTERISTICS (Pre and Post-Radiation)*
(V_{DD2} = 2.3 to 3.6V, 1 second DR pulse)

SYMBOL	PARAMETER	TEMP	MINIMUM	MAXIMUM	UNIT
V_{DR}	V_{DD1} for data retention	--	1.0	--	V
I_{DDR} [1]	Data retention current (per die)	-55°C	--	3	mA
		25°C	--	3	mA
		105°C	--	23.5	mA
t_{EFR} [1,2]	Chip deselect to data retention time	--	0	--	ns
t_R [1,2]	Operation recovery time	--	t_{AVAV1} t_{AVAV2}	--	ns

Notes:
* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.
1. En as shown all other inputs = V_{DD2} or V_{SS}.
2. Guaranteed by design neither tested nor characterized.

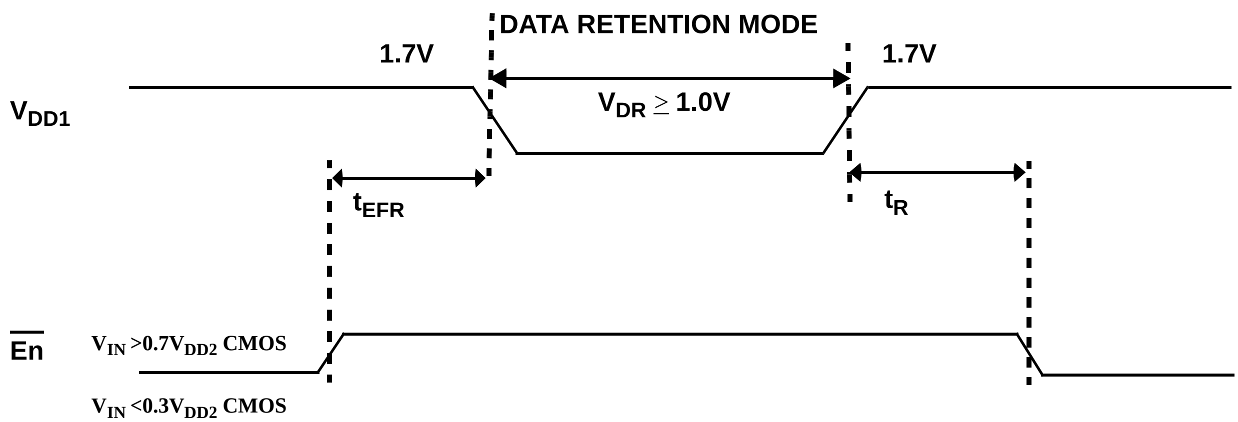
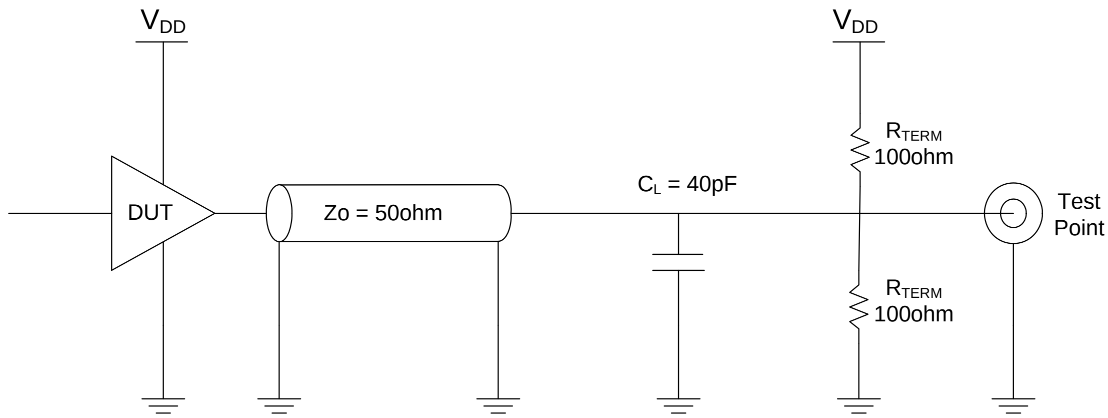
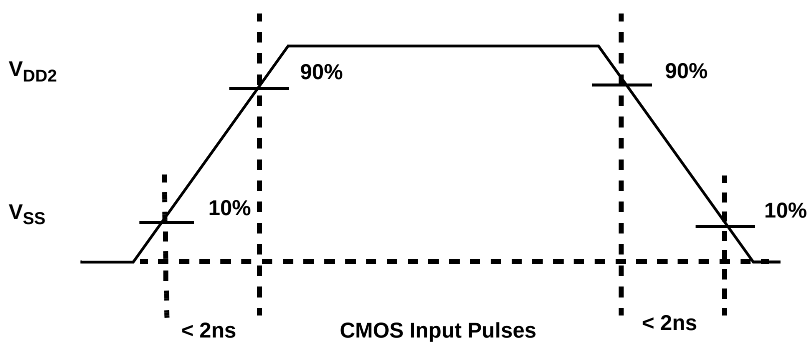


Figure 5. Low V_{DD} Data Retention Waveform





Notes:
1. Measurement of data output occurs at the low to high or high to low transition mid-point (i.e., CMOS input = $V_{DD2}/2$

Figure 6. AC Test Loads and Input Waveforms

PACKAGING

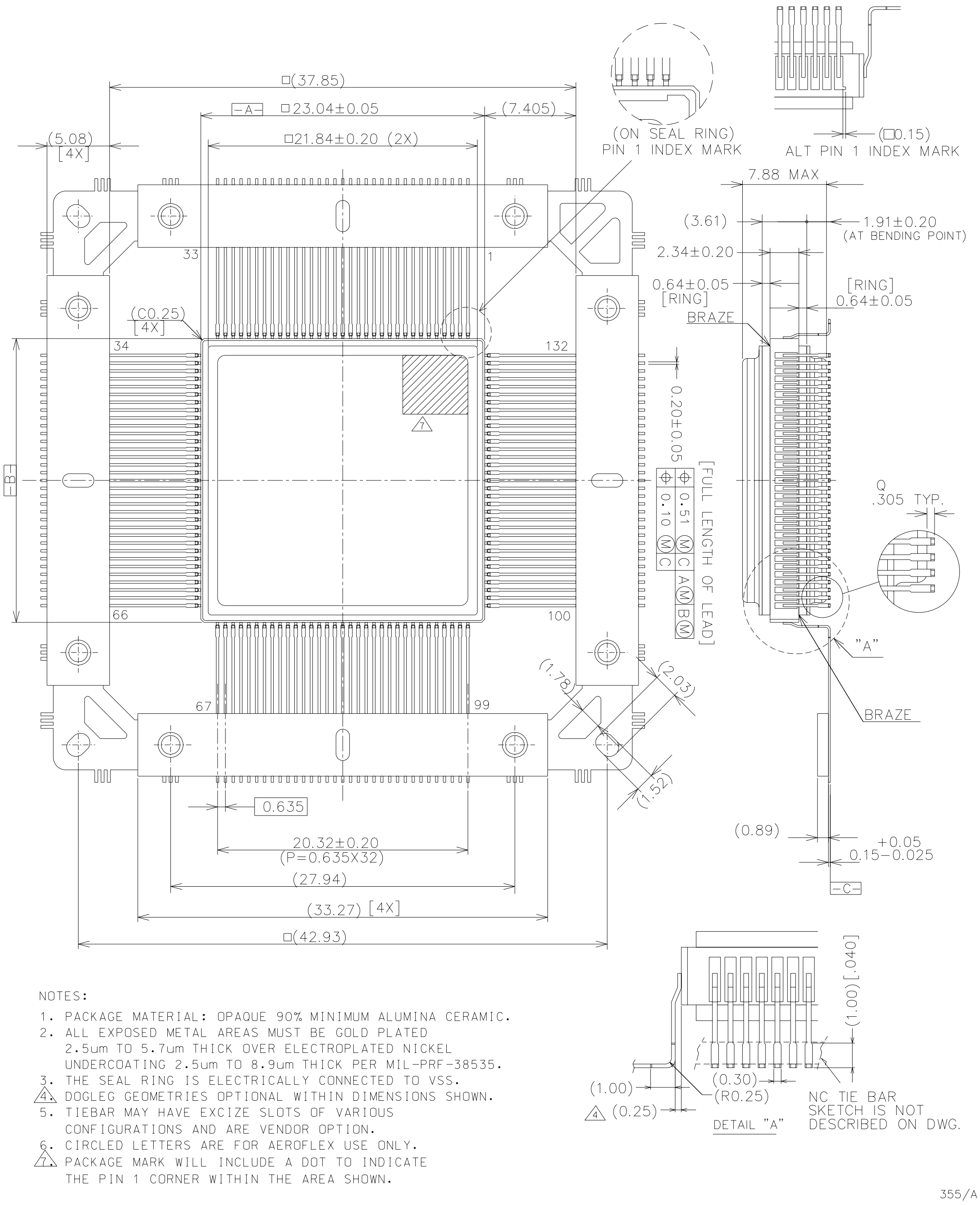


Figure 7. 132-Lead Side-Brazed Dual Cavity Ceramic Quad Flatpack

ORDERING INFORMATION

40Mbit (1Mx39) SRAM MCM
80Mbit (2Mx39) SRAM MCM
160Mbit (4Mx39) SRAM MCM

UT ****** - * * * * *

Lead Finish: **(Note 1)**
(C) = Gold

Screening: **(Notes 2, 3)**
(F) = HiRel Flow (Temperature Range: -55°C to +105°C)
(P) = Prototype Flow (Temperature Range: 25°C only)

Package Type:
(X) = 132-lead ceramic quad flatpack, side-brazed, dual cavit y

Access Time: **(Note 4)**
(21) = 20ns read / 10ns write access times, 40Mbit device type
(22) = 22ns read / 10ns writeaccess times, 80Mbit device type
(25) = 25ns read / 10ns write access times, 160Mbit device type

Device Type:
(8R1M39) = 40Mbit (1Mx39) SRAM MCM
(8R2M39) = 80Mbit (2Mx 39) SRAM MCM
(8R4M39) = 160Mbit (4Mx39) SRAM MCM

Notes:
1. Lead finish is "C" (Gold) only.
2. Prototype Flow per Aeroflex Manufacturing Flows Document. Devices are tested at 25°C only. Lead finish is GOLD "C" only. Radiation is neither tested nor guaranteed.
3. HiRel flow per Aeroflex Manufacturing Flows Document. Radiation is neither tested nor guaranteed.
4. Device option (21) applicable to 40Mbit device type only. Option (22) applicable to 80Mbit device type only. Option (25) applicable to 160Mbit device type only.

40Mbit (1Mx39) SRAM MCM: SMD
80Mbit (2Mx39) SRAM MCM: SMD
160Mbit (4Mx39) SRAM MCM: SMD

5962 * ***** ** * * *

Lead Finish: (Note 1)
(C) = Gold

Case Outline:
(X) = 132-lead ceramic quad flatpack, side brazed, dual cavity

Class Designator:
(Q) = QML Class Q
(V) = QML Class V (10205 and 10206 device options only)

Device Type: (Note 2)
(01) = Temperature Range (-55°C to +105°C)
(02) = Assembled to Aeroflex Q+ Flow (Temperature Range -55°C to +105°C)

Drawing Number:
(10205) = 40Mbit (1Mx39) SRAM MCM
(10206) = 80Mbit (2Mx39) SRAM MCM
(10207) = 160Mbit (4Mx39)SRAM MCM

Total Dose: (Note 3)
(R) = 100 krad(Si)

Federal Stock Class Designator: No options

Notes:
1. Lead finish is "C" (Gold) only.
2. Aeroflex’s Q+ assembly flow, as defined in section 4.2.2.d of the SMD, provides QML-Q product through the SMD that is manufactured with Aeroflex’s standard QML-V flow and has completed QML-V qualification per MIL-PRF-38535.
3. TID tolerance guarantee of 1E5 is tested in accordance with MIL-STD-883 Test Method 1019 (condition A and section 3.11.2) resulting in an effective dose rate of 1 rad(Si)/sec.

Aeroflex Colorado Springs - Datasheet Definition

Advanced Datasheet - Product In Development

Preliminary Datasheet - Shipping Prototype

Datasheet - Shipping QML & Reduced Hi-Rel

This product is controlled for export under the Export Administration Regulations (EAR), 15 CFR Parts 730-774. A license from the Department of Commerce may be required prior to the export of this product from the United States.

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DATA SHEET REVISION HISTORY

REV	Revision Date	Description of Change	Page(s)	Author
1.0.0	6/15	Added new datasheet format	All	Leslie
2.0.0	12/15	Added new Table 1, edited notes on Figures 4a and 4b, updated export disclaimer	3, 17,18, 25	Leslie

Low Power SRAM Read Operations

Table 1: Cross Reference of Applicable Products

Product Name:	Manufacturer Part Number	SMD #	Device Type	Internal PIC Number:*
4M Asynchronous SRAM	UT8R128K32	5962-03236	01 & 02	WC03
4M Asynchronous SRAM	UT8R512K8	5962-03235	01 & 02	WC01
16M Asynchronous SRAM	UT8CR512K32	5962-04227	01 & 02	MQ08
16M Asynchronous SRAM	UT8ER512K32	5962-06261	05 & 06	WC04/05
4M Asynchronous SRAM	UT8Q512E	5962-99607	05 & 06	WJ02
4M Asynchronous SRAM	UT9Q512E	5962-00536	05 & 06	WJ01
16M Asynchronous SRAM	UT8Q512K32E	5962-01533	02 & 03	QS04
16M Asynchronous SRAM	UT9Q512K32E	5962-01511	02 & 03	QS03
32M Asynchronous SRAM	UT8ER1M32	5962-10202	01 - 04	QS16/17
64M Asynchronous SRAM	UT8ER2M32	5962-10203	01 - 04	QS09/10
128M Asynchronous SRAM	UT8ER4M32	5962-10204	01 - 04	QS11/12
40M Asynchronous SRAM	UT8R1M39	5962-10205	01 & 02	QS13
80M Asynchronous SRAM	UT8R2M39	5962-10206	01 & 02	QS14
160M Asynchronous SRAM	UT8R4M39	5962-10207	01 & 02	QS15

* PIC = Aeroflex's internal Product Identification Code

1.0 Overview

The purpose of this application note is to discuss the Aeroflex SRAMs low power read architecture and to inform users of the affects associated with the low power read operations.

2.0 Low Power Read Architecture

The aforementioned Aeroflex designed SRAMs all employ an architecture which reduces power consumption during read accesses. The architecture internally senses data only when new data is requested. A request for new data occurs anytime the chip enable device pin is asserted, or any of the device address inputs transition states while the chip enable is asserted. A trigger is generated and sent to the sensing circuit anytime a request for new data is observed. Since several triggers could occur simultaneously, these triggers are wire-ORed to result in a single sense amplifier activity for the read request. This design method results in less power consumption than designs that continually sense data. Aeroflex's low power SRAMs listed above activate the sensing circuit for approximately 5ns whenever and access is requested, thereby, significantly reducing active power.

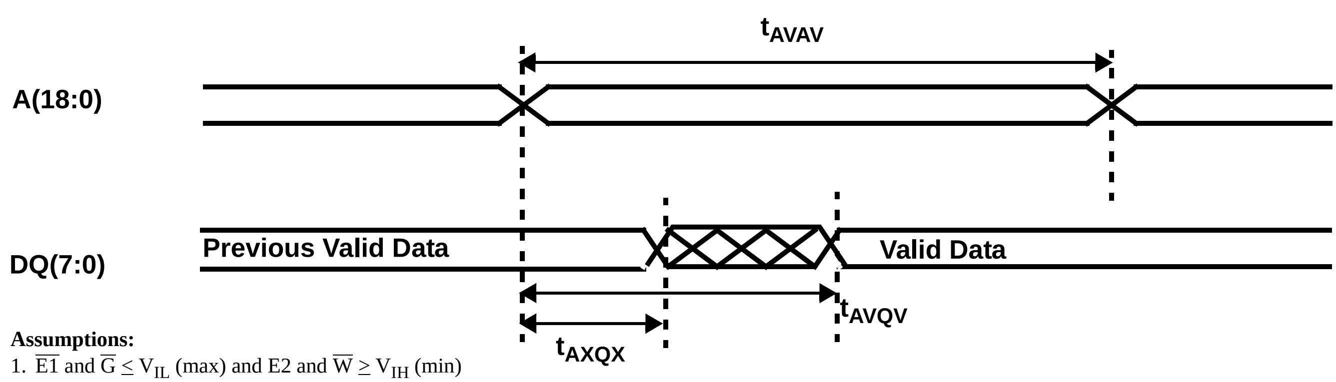
2.1 The SRAM Read Cycles.

The data sheets for all the devices noted in Table #1 discuss three methods for performing a read operation. The two most common methods for reading data are an Address Access and a Chip Enabled-Controlled Access. The third access discussed is the Output Enable-Controlled Access. The sequence at which control lines and address inputs are toggled determines which cycle is considered relevant. As discussed in section 2.0, an assertion of chip enable or any address transition while chip enable is asserted, initiates a read cycle. If the device chip enable is asserted prior to any address input transitions, then the read access is considered an Address Access. By keeping the device enabled and repeatedly switching address locations, the user retrieves all data of interest. A Chip Enable-Controlled Access occurs when the address signals are stable prior to asserting the chip enable. The Output Enabled-Controlled Access requires that either an Address Access or Chip Enable-Controlled Access has already been performed and the data is waiting for the Output Enable pin to assert, driving data to the device I/O pins.

The subsequent read cycle verbiage and diagrams are based on the Aeroflex UT8R512K8 data sheet. The number of control, input, and I/O pins will vary across the products listed in Table 1. The basic design family functionality for read operations is common among all the devices.

2.1.0 Address Access Read Cycle

The Address Access is initiated by a change in address inputs while the chip is enabled with $\overline{G}$ asserted and $\overline{W}$ deasserted. Valid data appears on data outputs DQ(7:0) after the specified t_{AVQV} is satisfied. Outputs remain active throughout the entire cycle. As long as chip enable and output enable are active, the address inputs may change at a rate equal to the minimum read cycle time (t_{AVAV}).



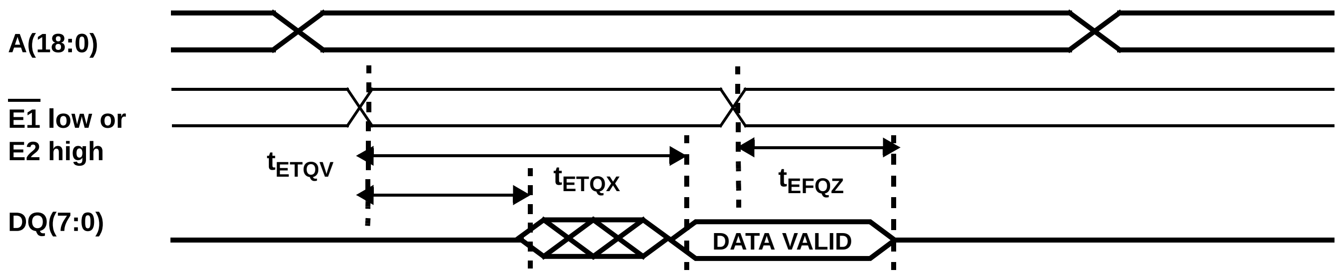
Assumptions:
1. $\overline{E1}$ and $\overline{G} \leq V_{IL}$ (max) and E2 and $\overline{W} \geq V_{IH}$ (min)

Note: No time references are relevant with respect to Chip Enable(s). Chip Enable(s) is assumed to be asserted.

SRAM Read Cycle 1: Address Access

2.1.1 Chip Enable-Controlled Read Cycle

The Chip Enable-controlled Access is initiated by $\overline{E1}$ and E2 going active while $\overline{G}$ remains asserted, $\overline{W}$ remains deasserted, and the addresses remain stable for the entire cycle. After the specified t_{ETQV} is satisfied, the eight-bit word addressed by A(18:0) is accessed and appears at the data outputs DQ(7:0).



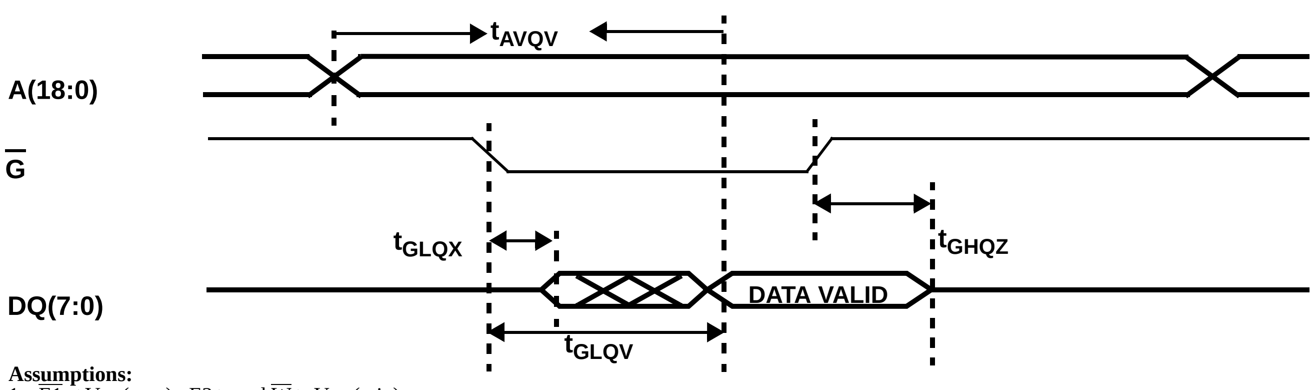
Assumptions:
1. $\overline{G} \leq V_{IL}$ (max) and $\overline{W} \geq V_{IH}$ (min)

Note: <u>No specification is given for address set-up time with respect to chip enable assertion. The read cycle description states that addresses are to remain stable for the entire cycle. Address set-up time relative to chip enable is assumed to be 0ns minimum.</u>

SRAM Read Cycle 2: Chip Enable Access

2.1.1 Output Enabled-Controlled Read Cycle

The Output Enable-controlled Access is initiated by $\overline{G}$ going active while $\overline{E1}$ and E2 are asserted, $\overline{W}$ is deasserted, and the addresses are stable. Read access time is t_{GLQV} unless t_{AVQV} or t_{ETQV} have not been satisfied.



Assumptions:
1. $\overline{E1} \leq V_{IL}$ (max) , E2 > and $\overline{W} \geq V_{IH}$ (min)

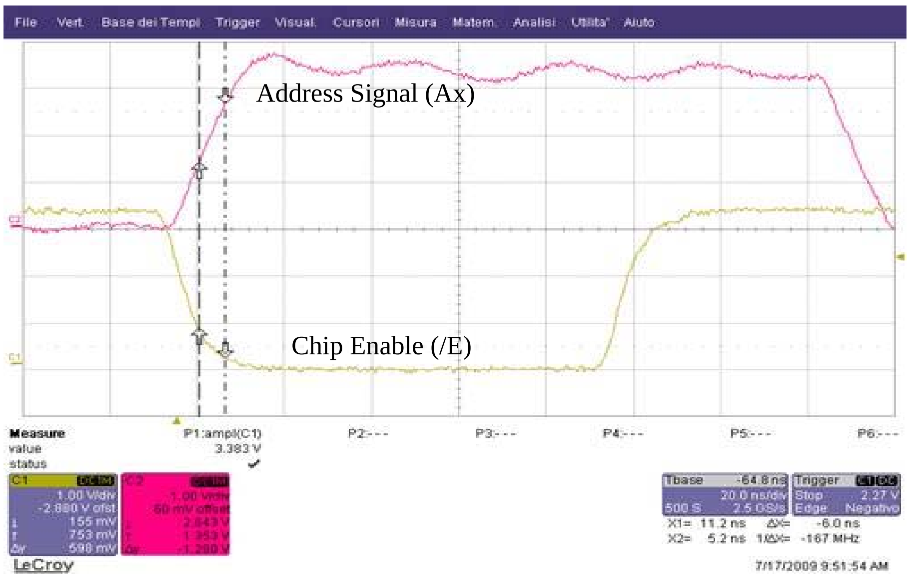
SRAM Read Cycle 3: Output Enable Access

<u>3.0 Low Power Read Architecture Timing Consideration</u>

The low power read architecture employed by Aeroflex designed SRAMs results in significant power reduction, especially in applications with longer than minimum read cycle times. However, this type of architecture is responsive to excessive input signal skew when device addressing and chip enable assertion occur simultaneously. Signal skew of greater than 4-5ns between all of the read triggering activities is sufficient to start another read cycle.

3.1 Simultaneous Control and Address Switching

Simultaneous switching of controls and address pins, alone, is not a problem; excessive skew between them is the concern. Consider the application where several SRAM devices are connected to the same memory bus. The address bus is commonly connected to all the devices, but the chip enable pin is singularly connected to each individual SRAM. This configuration results in a loading difference between the address inputs and the chip enable. This lightly loaded chip enable propagates to the memory more quickly than the heavily loaded address lines. The oscilloscope capture of Figure #1 is the actual timing of an application which had intermittent data errors due to address transitions lagging chip enable.



- Timing shown from VIL (yellow trace /CS) and VIH (pink for address signal) as delta X = 6ns. Even at actual internal gate switching point (~ VDD/2), the skew is still around 6ns.

Figure #1 SRAM Signal Capture

The signal transitions in the scope plot of Figure #1 appear to be fairly coincidental. A closer look however, reveals the chip enable signal actually starts and reaches V_{IL} approximately 6ns before the address signal reaches V_{IH}. Even at one half V_{DD} (closer to actual logical gate switching of the inputs), the delta in signal times is still approximately 6ns.

Simultaneous switching of controls and address inputs is not recommended for a couple of reasons. The first is the previously described signal skew sensitivity between controls and/or address inputs. The second reason is that activating all the controls and address inputs simultaneously results in peak instantaneous current consumption. This condition causes maximum strain to the power decoupling. Chip Enable activates address decoding circuits, address switching introduces input buffer switching current, and output enable assertion turns on all the device output drivers. Peforming all three simultaneously results in worst case transient current demand by the memory.

3.1.0 Technical Overview of Skew Sensitivity

Recall from section 2.0 that any activity requesting new data causes a read trigger. The triggers are wire-ORed together. In order to meet the faster access times demanded by today’s applications, the ORed trigger only exists during the first 4-5ns of the read cycle. Since the slowest of the address transitions occurs more than 5ns after the initiation of the read activity, a second read activity is initiated. The sensing circuit does not have time to normalize before the second read activity has started. For this reason a Chip Enable-Controlled read cycle requires that address inputs remain stable for the entire cycle. Infrequent and random sensing errors can result if the bit columns are continually pulled to one state then quickly requested to sense the opposite state. Another effect of the low power read architecture that differs from previous generation designs (those that continually sense for data) is that the bit line will not be sensed again until another read triggering event occurs. If another read trigger event (chip enable assertion and/or address change) does no occur for a particular address, the incorrect data remains at the outputs.

4.0 Summary and Conclusion

The Aeroflex SRAMs in Table #1 all employ a low power consumption read architecture. Power is conserved by sensing data only when new data is requested. A request occurs anytime chip enable is asserted or any address input signal transitions while chip enable is asserted. The data sheets for the SRAMs listed in Table #1 do not explicitly define the case of simultaneous switching of address and control signals during read operations. Data sheet read cycle descriptions indicate that control inputs are established prior to address changes, and address inputs are stable prior to control assertions. Simultaneous switching of addresses and controls is tolerable, when the skew between all input signals is < 4ns. For designs that must employ the simultaneous activation of address and control signals, two important issues should be considered by the designer. The first is the input signal skew sensitivity of the low power read architecture discussed by this application note. The second is the instantaneous current consumption that results from simultaneous access methods. Aeroflex recommends the use of only one read access method at a time. If multiple read accesses (simultaneous chip enable assertion and address switching) cannot be avoided, then Aeroflex recommends that the chip enable signal be delayed until all addresses have completed transitions.