Standard Products

UT8MR8M8 64Megabit Non-Volatile MRAM

Datasheet

January 2016

The most important thing we build is trust

FEATURES

- Single 3.3-V power supply
- Fast 50ns read/write access time
- Functionally compatible with traditional asynchronous SRAMs
- Equal address and chip-enable access times
- HiRel temperature range (-40°C to +105°C)
- Automatic data protection with low-voltage inhibit circuitry to prevent writes on power loss
- CMOS and TTL compatible
- Data non-volatile for > 20 years (-40°C to +105°C)
- Read/Write endurance: Unlimited for 20 years (-40°C to +105°C)
- 64-pin ceramic flatpack package
- Operational environment:
  - Total dose: 1 Mrad(Si)
  - SEL Immune: 112 MeV-cm^2/mg @125°C
  - SEU Immune: Memory Cell 112 MeV-cm^2/mg @25°C
- Standard Microelectronics Drawing (SMD) - 5962-13207
  - QML Q, Q+, and V

INTRODUCTION

The Cobham (formerly Aeroflex) 64Megabit Non-Volatile magnetoresistive random access memory (MRAM) is a high-performance memory multichip module (MCM) compatible with traditional asynchronous SRAM operations, organized as either four 2M words by 8 bits or one 8M words by 8 bits.

The MRAM is equipped with five chip enables (/En), a single write enable (/W), and a single output enable (/G) pins, allowing for significant system design flexibility without bus contention. Data is non-volatile for > 20 years at temperature and data is automatically protected against power loss by a low voltage write inhibit.

The 64Mb MRAM is designed specifically for operation in HiREL environments. As shown in Table 4, the magneto-resistive bit cells are immune to Single Event Effects (SEE). To guard against transient effects, an Error Correction Code (ECC) is included within the device. ECC check bits are generated and stored within the MRAM array during writes. The MBE pin identifies that ECC logic has detected two bit errors during the current read cycle.

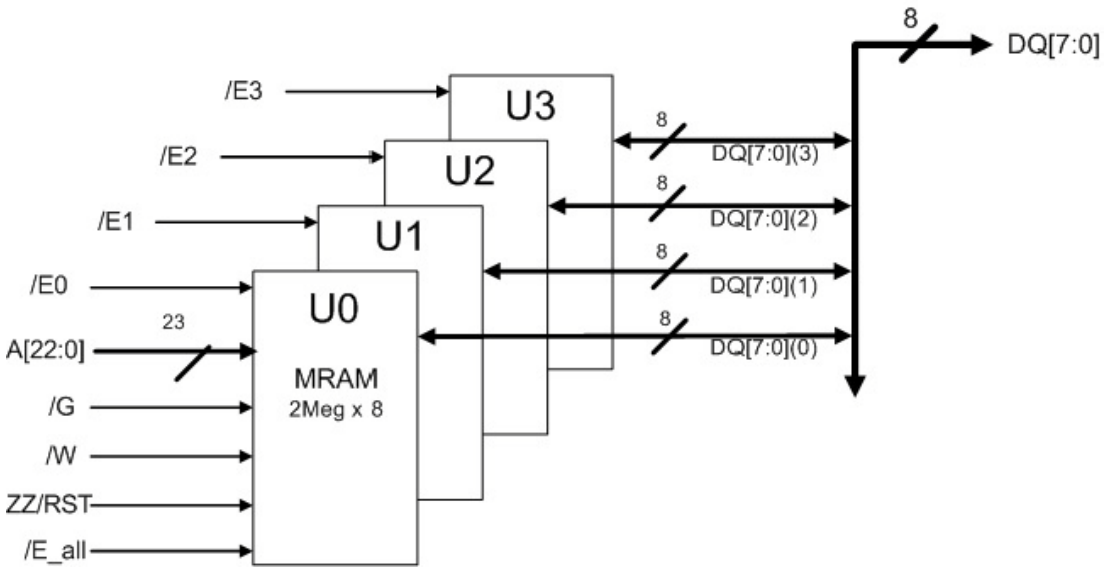


Figure 1. UT8MR8M8 MRAM Block Diagram

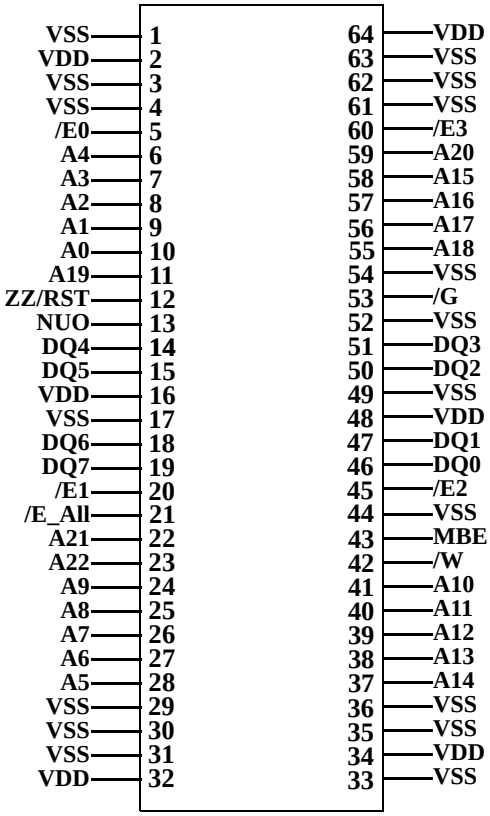


Figure 2. 40ns MRAM Pinout (64)

DEVICE OPERATION

The UT8MR8M8 has control inputs called Chip Enable (E[3:0]), Chip Enable All (/E_ALL), Write Enable (/W), Output Enable (/G), and sleep/reset mode (ZZ/RST); 23 address inputs, A[22:0]; eight bidirectional data lines, DQ[7:0]; and a Multi-bit Error Flag (MBE). /E[3:0] controls device selection, active, and standby modes. Asserting /E[3:0] enables the device, causes IDD to rise to its active value, and decodes the 21 address inputs, A[20:0], to select one of 16,777,216 words in the memory. **Note:** Only one Chip Enable may be active at any time. Asserting / E_ALL allows the device to be addressed as a single, 64Mb memory using address bits A21 and A22 to decode and select 1 of 4 MRAM die. /W controls read and write operation. During a read cycle, /G must be asserted to enable the outputs. ZZ/RST controls the sleep/reset mode operation and provides device reset capability. Enabling sleep/reset mode causes all other inputs to be don't cares. ZZ/RST places all die into internal low power even while system power is still applied to V_{DD}. The MBE pin is an open drain in which when pulled down, it identifies that ECC logic has detected two bit errors during the current read cycle. It allows for wired-or of multiple MBE when using multiple MRAMs.

PIN NAMES

Table 1. 8M x 8 Pin Functions

Signal Name	Function
A[22:0]	Address Input
/E[3:0][1]	Chip Enable
/E_All	Chip Enable All
/W	Write Enable
/G	Output Enable
DQ[7:0]	Data I/O
VDD	Power Supply
VSS	Ground
ZZ/RST	Deep Power Down/Reset (Internal pull down)
MBE[2]	Multi-Bit Error Flag
NUO	Not used output Do not connect Driven internally

***Notes:**
1.Only one /E[3:0] pin may be active at any time.
2. MBE pin is not functionally tested for prototypes.

Table 2. Chip Enable Functions Table

/E_ALL	/E_0	/E_1	/E_2	/E_3	A22	A21	Comment
0	1	1	1	1	0	0	MRAM Die 0 Enabled
0	1	1	1	1	0	1	MRAM Die 1 Enabled
0	1	1	1	1	1	0	MRAM Die 3 Enabled
0	1	1	1	1	1	1	MRAM Die 2 Enabled
1	0	1	1	1	X	X	MRAM Die 0 Enabled
1	1	0	1	1	X	X	MRAM Die 1 Enabled
1	1	1	0	1	X	X	MRAM Die 2 Enabled
1	1	1	1	0	X	X	MRAM Die 3 Enabled

***Note:** Only one /E[3:0] pin may be active at any time.

Table 3. Device Operation Truth Table

ZZ/ RST	/E[3:0]*	/G	/W	Mode	VDD Current	DQ[7:0]
H	X	X	X	Deep Sleep/ Reset Mode	Q_{IZZ}	HI-Z
L	H	X	X	Not Selected	Q_{IDD}	HI-Z
L	L	H	H	Output Disabled	I_{DDR}	HI-Z
L	L	L	H	Byte Read	I_{DDR}	D_{OUT}
L	L	X	L	Byte Write	I_{DDW}	D_{IN}

***Note:** Only one /E[3:0] pin may be active at any time.

READ CYCLE

A combination of /W greater than V_{IH} (min) and a single /En less than V_{IL} (max) defines a read cycle. Read access time is measured from the latter of chip enable, output enable, or valid address to valid data output.

MRAM Read Cycle 1, the Address Access in Figure 4a, is initiated by a change in address inputs after a single /En is asserted, /G asserted and /W deasserted. Valid data appears on data outputs DQ[7:0] after the specified t_{AVQV} is satisfied. Outputs remain active throughout the entire cycle. As long as a single chip enable and output enable are active, the address inputs may change at a rate equal to the minimum read cycle time (t_{AVAV}).

MRAM Read Cycle 2, the Chip Enable-controlled Access in Figure 4b, is initiated by a single /En going active while /G remains asserted, /W remains deasserted, and the addresses remain stable for the entire cycle. After the specified t_{ELQV} is satisfied, the eight-bit word addressed by A[20:0] is accessed and appears at the data outputs DQ[7:0].

WRITE CYCLE

A combination of /W and a single /En less than V_{IL}(max) defines a write cycle. The state of /G is a “don’t care” for a write cycle. The outputs are placed in the high-impedance state when either /G is greater than V_{IH}(min), or when /W is less than V_{IL}(max).

Write Cycle 1, the Write Enable-controlled Access in Figure 5a, is defined by a write terminated by /W going high, with a single /En still active. The write pulse width is defined by t_{WLWH} when the write is initiated by /W, and by t_{ETWH} when the write is initiated by a single /En. Unless the outputs have been previously placed in the high-impedance state by /G, the user must wait t_{WLQZ} before applying data to the nine bidirectional pins DQ[7:0] to avoid bus contention.

Write Cycle 2, the Chip Enable-controlled Access in Figure 5b, is defined by a write terminated by a single /En going inactive. The write pulse width is defined by t_{WLEH} when the write is initiated by /W, and by t_{ELEH} when the write is initiated by a single /En going active. For the /W initiated write, unless the outputs have been previously placed in the high-impedance state by /G, the user must wait t_{WLQZ} before applying data to the eight bidirectional pins DQ[7:0] to avoid bus contention.

OPERATIONAL ENVIRONMENT

The UT8MR8M8 MRAM incorporates special design and layout features which allows operation in harsh environments.

Table 4. Operational Environment Design Specifications

PARAMETER	LIMIT	UNITS
TID	1	Mrad(Si)
SEL Immunity[1]	≤ 112	MeV-cm^2/mg
SEU Memory Cell Immunity[2]	≤ 112	MeV-cm^2/mg

Notes:

1. SEL test performed at V_{DD} = 3.6V and temperature = 125^{o}C.
2. SEU test performed at V_{DD} = 3.0V and unpowered at room temperature.

POWER UP AND POWER DOWN SEQUENCING

The MRAM is protected from write operations whenever V_{DD} is less than V_{WI}. As soon as V_{DD} exceeds V_{DD}(min), there is a startup time of 2 ms before read or write operations can start. This time allows memory power supplies to stabilize. The /En and /W control signals should track V_{DD} on power up to V_{DD}-0.2 V or V_{IH} (whichever is lower) and remain high for the startup time. In most systems, this means that these signals should be pulled up with a resistor so the signal remains high if the driving signal is Hi-Z during power up. Any logic that drives /En and /W should hold the signals high with a power-on reset signal for longer than the startup time. During power loss or brownout where V_{DD} goes below V_{WI}, writes are protected and a startup time must be observed when power returns above V_{DD}(min).

The MRAM supports sleep/reset mode operation using the ZZ/RST control pin. To enter sleep mode/reset, ZZ/RST must be pulled high. The device will enter sleep/reset mode within 40ns. In order to exit sleep/reset mode, /En and /W must be high before ZZ/RST is pulled low. As soon as ZZ/RST is driven low, the user must allow 100us before performing any other operation in order for the device to properly initialize. Aeroflex recommends designing a system level method to toggle the ZZ/RST pin in order to reset the MRAM device.

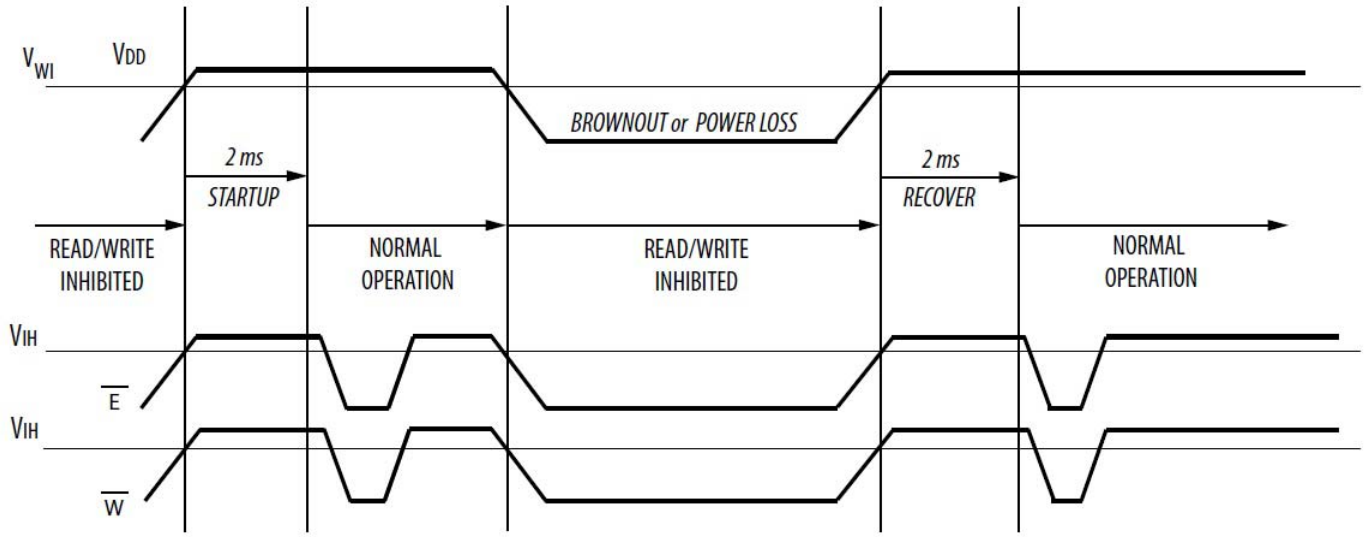


Figure 4. UT8MR2M8 Power Up and Power Down Sequencing Diagram

MBE PIN FUNCTIONALITY AND SEQUENCING

The 64M MRAM is a Multi-Chip Module (MCM) made up of four 16M MRAM die. Each die has its own open drain MBE pin and these pins are wire or connected within the UT8MR8M8 package. The MBE output is not defined after power up or after coming out of sleep until the MRAM is enabled for the first time. In order for the MBE pin to have guaranteed valid data, all die within the package must be accessed. This can be accomplished by toggling the four separate enable pins (/En[0:3]) , or by toggling through A[22:21] with /En_ALL held low. See Figures 5 and 6.

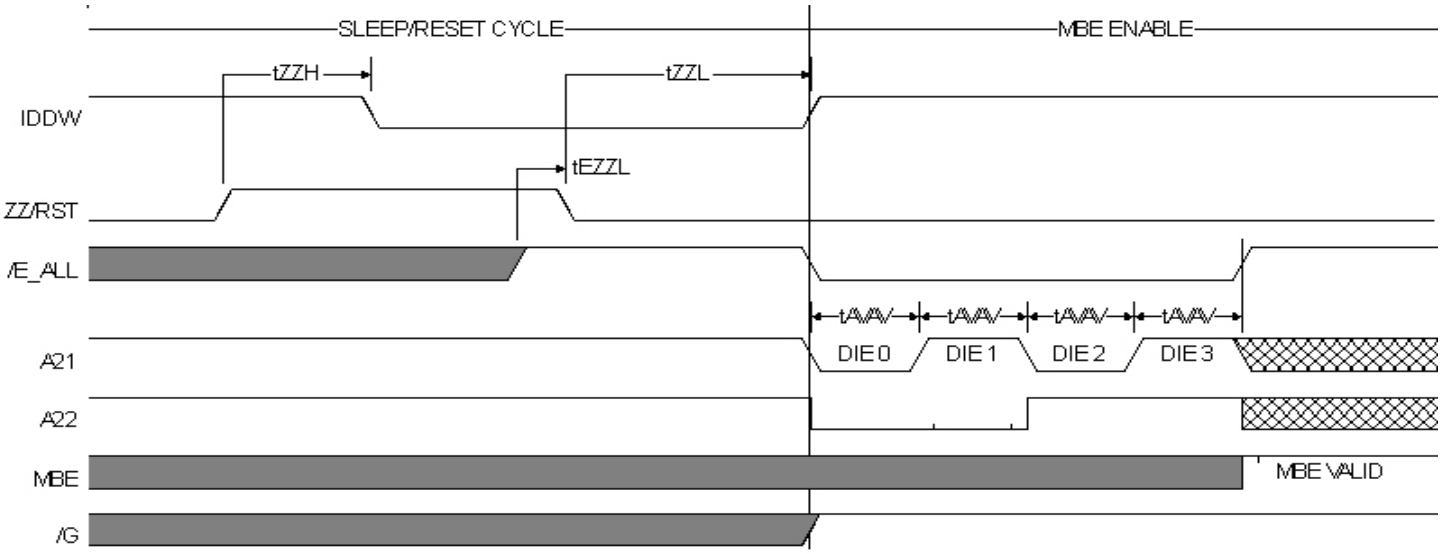


Figure 5. Post Reset MBE Enable using A21, A22, & /E_All

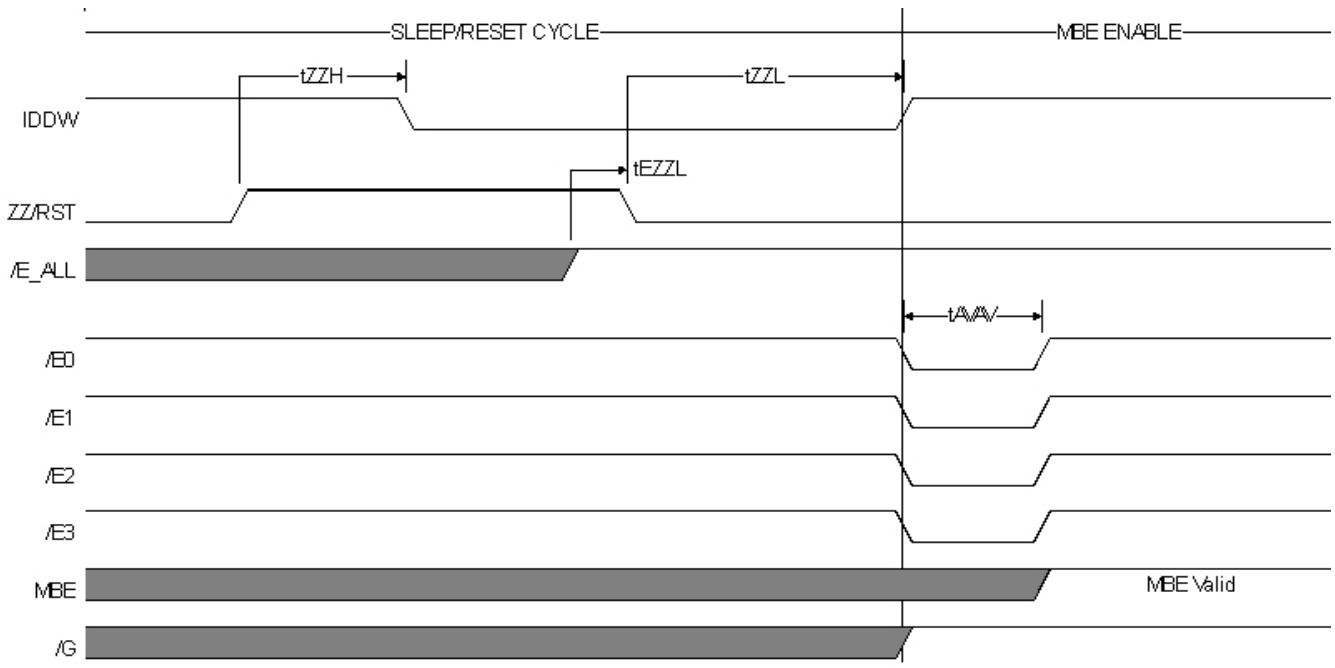


Figure 6. Post Reset MBE enable using enable pins /E[3:0]

ABSOLUTE MAXIMUM RATINGS[1]

(Referenced to V_{SS})

The device contains protection against magnetic fields. Precautions should be taken to avoid device exposure of any magnetic field intensity greater than specified.

SYMBOL	PARAMETER	VALUE	UNIT
V_{DD}	Supply Voltage[2]	-0.5 to 4.3	V
V_{IN}	Voltage on any pin[2]	-0.5 to V_{DD}+0.5	V
I_{IO}	DC I/O current per pin @ T_J = 125° for 20yrs	± 20	mA
P_D	Package power dissipation[3]	4	W
T_J	Maximum junction temperature	+150	^oC
θ_{JC}	Thermal resistance junction to case – Single Die	5	$^oC/W$
T_{STG}	Storage temperature	-65 to +125	^oC
ESD_{HBM}	ESD	>2000	V
H_{max_write}	Maximum magnetic field during write	8000	A/m
H_{max_read}	Maximum magnetic field during read or standby	8000	A/m

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to excessive voltages or magnetic fields could affect device reliability.
2. All voltages are referenced to V_{SS}.
3. Power dissipation capability depends on package characteristics and use environment

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS
T_C	Operating case temperature	-40^{o}C to +105^{o}C
V_{DD}	Operating supply voltage	3.0V to 3.6V
V_{WI}	Write inhibit voltage	2.5V to 3.0V[1]
V_{IH}	Input high voltage	2.2V to V_{DD}+0.3V
V_{IL}	Input low voltage	V_{SS}-0.3V to 0.8V

Notes:

1. After power up or if V_{DD} falls below V_{WI}, a waiting period of 2 ms must be observed, and /En and /W must remain high for 2 ms. Memory is designed to prevent writing for all input pin conditions if V_{DD} falls below minimum V_{WI}.

DC ELECTRICAL CHARACTERISTICS (Pre and Post-Radiation)*

V_{DD} = 3.0V to 3.6V; Unless otherwise noted, Tc is per the temperature ordered

SYMBOL	PARAMETER	CONDITION		MIN	MAX	UNIT
V_{IH}	High-level input voltage			2.0		V
V_{IL}	Low-level input voltage				0.8	V
V_{OL1}	Low-level output voltage	I_{OL} = 4mA,V_{DD} =V_{DD} (min)			0.4	V
V_{OL2}	Low-level output voltage	I_{OL} = + 100µA,V_{DD} =V_{DD} (min)			V_{SS}+0.2	V
V_{OH1}	High-level output voltage	I_{OH} = -4mA,V_{DD} =V_{DD} (min)		2.4		V
V_{OH2}	High-level output voltage	I_{OH} = -100µA,V_{DD} =V_{DD} (min)		V_{DD}-0.2		V
C_{IN}[1]	Input capacitance	f = 1MHz @ 0V			50	pF
C_{IO}[1]	Bidirectional I/O capacitance	f = 1MHz @ 0V			60	pF
I_{IN}	Input leakage current	V_{IN} = V_{DD} and V_{SS}		-1	+1	µA
I_{INZZ}	Input leakage current ZZ/RST	V_{IN} = V_{DD} and V_{SS}		-0.25	0.25	mA
I_{OZ}	Three-state output leakage current	V_O = V_{DD} and V_{SS}, V_{DD} = V_{DD} (max) /G = V_{DD} (max)		-1	+1	µA
I_{OS}[2, 3]	Short-circuit output current	V_{DD} = V_{DD} (max), V_O = V_{DD} V_{DD} = V_{DD} (max), V_O = V_{SS}		-100	+100	mA
I_{DDR}	Active read supply current	Read mode f = max (I_{OUT} = 0mA; V_{DD} = max)			140	mA
I_{DDW}	Active write supply current	Write mode f = 10 MHz (V_{DD} = max)			140	mA
Q_{IDD}	Quiescent supply current	CMOS leakage current (/E = V_{DD}; all other inputs equal V_{SS} or V_{DD}; V_{DD} = max)	-40°C +25°C		30	mA
			+105°C		35	mA
Q_{IZZ}[4]	Deep power down and reset supply current	CMOS leakage current (/E = V_{DD}; all other inputs equal V_{SS} or V_{DD}; V_{DD} = max)			1	mA

Notes:

* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1. Measured only for initial qualification and after process or design changes that could affect input/output capacitance.
2. Supplied as a design limit but not guaranteed or tested.
3. Not more than one output may be shorted at a time for maximum duration of one second.
4. Allow 100µs to exit sleep/reset mode before performing any other operation.

AC CHARACTERISTICS READ CYCLE[1] (Pre and Post-Radiation)*

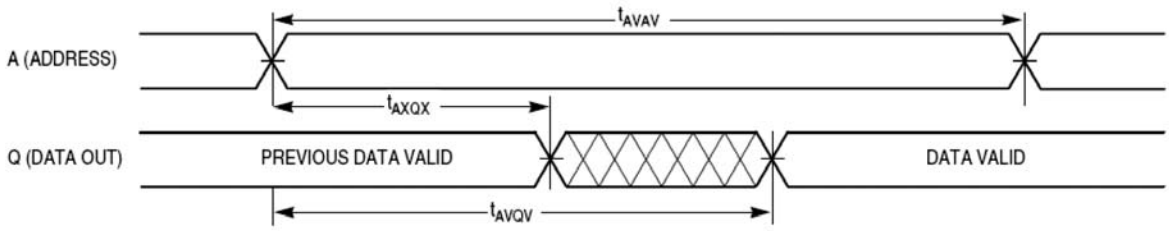
V_{DD} = V_{DD} (min); Unless otherwise noted, Tc is per the temperature ordered

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{AVAV}	Read cycle time	50		ns
t_{AVQV}	Address access time		50	ns
t_{ELQV}[2]	Enable access time		50	ns
t_{GLQV}	Output enable access time		25	ns
t_{AXQX}	Output hold from address change	3		ns
t_{ELQX}[3]	Enable low to output active	3		ns
t_{GLQX}[3]	Output enable low to output active	0		ns
t_{EHQZ}[3]	Enable high to output Hi-Z	0	15	ns
t_{GHQZ}[3]	Output enable high to output Hi-Z	0	15	ns

Notes:

* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1. /W is high for read cycle. Power supplies must be properly grounded and decoupled, and bus contention conditions must be minimized or eliminated during read or write cycles.
2. Address valid before or at the same time /En goes low.
3. Transition is measured at +/-400mV from the steady-state voltage.



NOTES:
Device is continuously selected (/En ≤ V_{IL}, $\overline{G}$ ≤ V_{IL}).

Figure 7a. MRAM Read Cycle 1

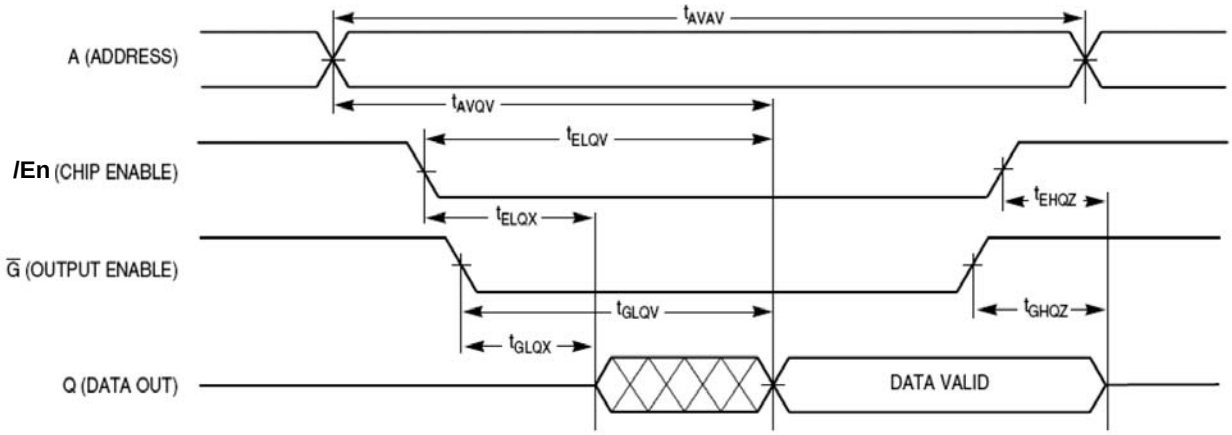


Figure 7b. MRAM Read Cycle 2

AC CHARACTERISTICS /W CONTROLLED WRITE CYCLE (Pre and Post-Radiation)*

V_{DD}= V_{DD} (min); Unless otherwise noted, Tc is per the temperature ordered.

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{AVAV}[2]	Write cycle time	50		ns
t_{AVWL}	Address set-up time	0		ns
t_{AVWH}	Address valid to end of write (/G high)	28		ns
t_{AVWH}	Address valid to end of write (/G low)	28		**ns**
t_{WLWH} t_{WLEH}	Write pulse width (/G high or low)	28		ns
t_{DVWH}	Data valid to end of write	10		ns
t_{WHDX}	Data hold time	0		ns
t_{WLQZ}[3]	Write low to data Hi-Z	0	15	ns
t_{WHQX}[3]	Write high to output active	3		ns
t_{WHAX}	Write recovery time	16		ns

Notes:

* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1. All write occurs during the overlap of /En low and /W low. Power supplies must be properly grounded and decoupled, and bus contention conditions must be minimized or eliminated during read or write cycles. If /G goes low at the same time or after /W goes low, the output will remain in a high impedance state.
2. All write cycle timings are referenced from the last valid address to the first transition address.
3. Transition is measured +/-400mV from the steady-state voltage.

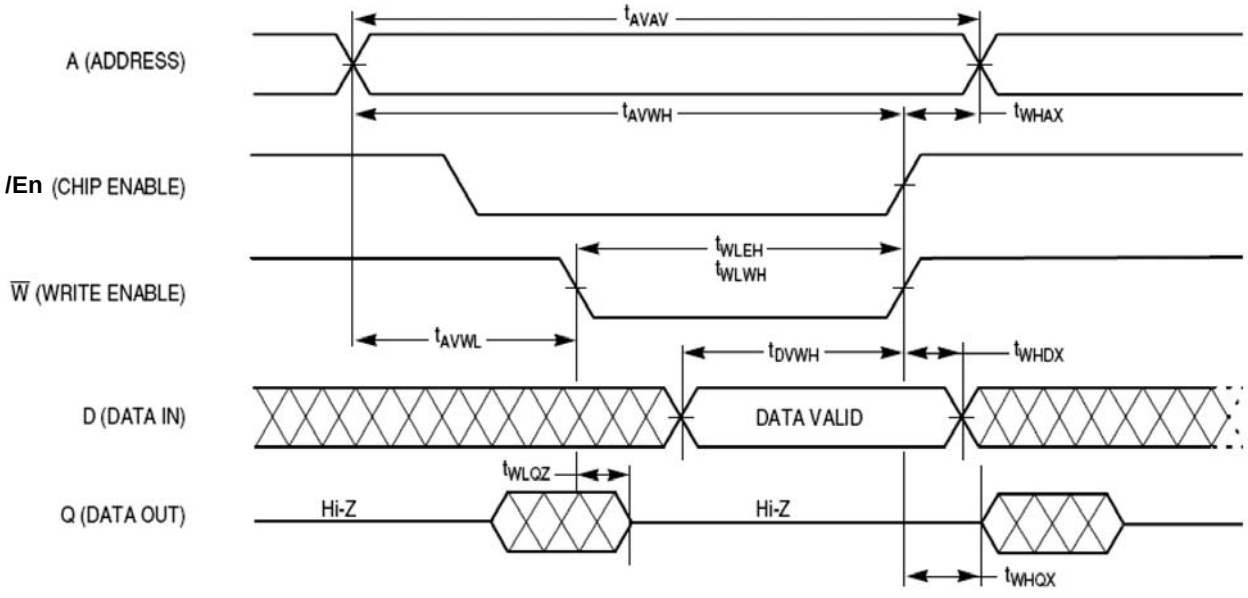


Figure 8a. MRAM Write Cycle 1 (/W Controlled Access)

AC CHARACTERISTICS /En CONTROLLED WRITE CYCLE[1] (Pre and Post-Radiation)*

V_{DD}= V_{DD} (min); Unless otherwise noted, Tc is per the temperature ordered.

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{AVAV}[2]	Write cycle time	50		ns
t_{AVEL}	Address set-up time	0		ns
t_{AVEH}	Address valid to end of write (/G high)	28		ns
t_{AVEH}	Address valid to end of write (/G low)	28		**ns**
t_{ELEH} t_{ELWH}	Enable to end of write (/G high)	28		ns
t_{ELEH}[3] t_{ELWH}[3]	Enable to end of write (/G low)	28		ns
t_{DVEH}	Data valid to end of write	10		ns
t_{EHDX}[4]	Data hold time	0		ns
t_{EHAX}[4]	Write recovery time	16		ns

Notes:

* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1. All write occurs during the overlap of /En low and /W low. Power supplies must be properly grounded and decoupled, and bus contention conditions must be minimized or eliminated during read or write cycles. If /G goes low at the same time or after /W goes low, the output will remain in a high impedance state.
2. All write cycle timings are referenced from the last valid address to the first transition address.
3. If /En goes low at the same time or after /W goes low, the output will remain in a high-impedance state. If /En goes high at the same time or before /W goes high, the output will remain in a high-impedance state.
4. Transition is measured +/-400mV from the steady-state voltage.

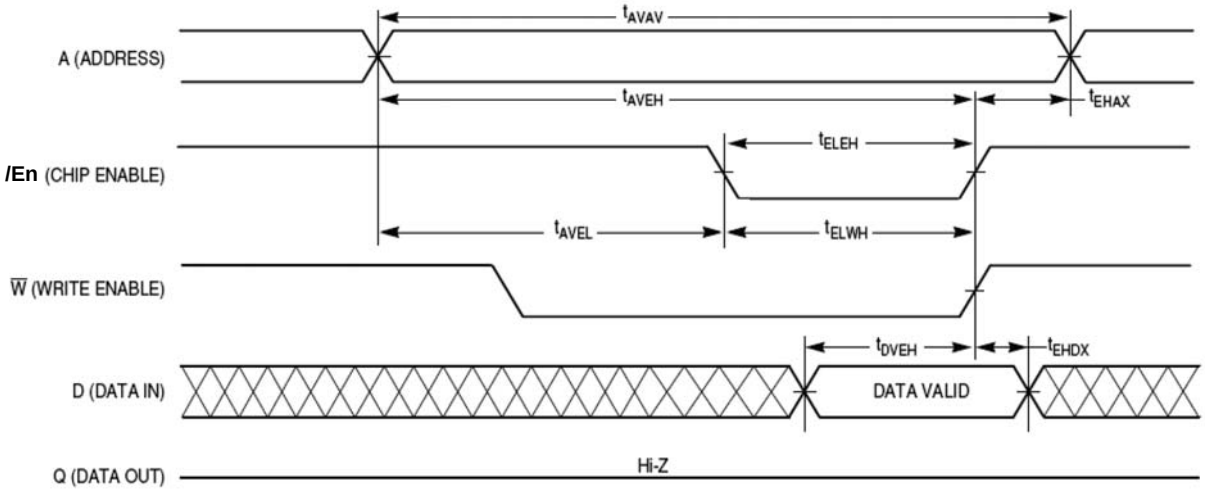


Figure 8b. MRAM Write Cycle 2 (/En Controlled)

AC CHARACTERISTICS SLEEP/RESET MODE (Pre and Post-Radiation)*

V_{DD}= V_{DD} (min); Unless otherwise noted, Tc is per the temperature ordered.

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{ZZL}[1,3]	Sleep/reset mode exit delay		100	µs
t_{ZZH}[2,3]	Sleep/reset mode access time	50		ns
t_{EZZ}[3]	Sleep/reset mode exit setup time	0		ns
t_{ZZS}[3]	Sleep/reset mode settle time		200	µs

Notes:

* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1. /En and /W must be high when ZZ/RST is pulled low in order to exit sleep/reset mode.
2. ZZ/RST must be high for 40ns in order to enter sleep/reset mode.
3. Parameters are supplied as a design limit, but are not tested nor guaranteed.

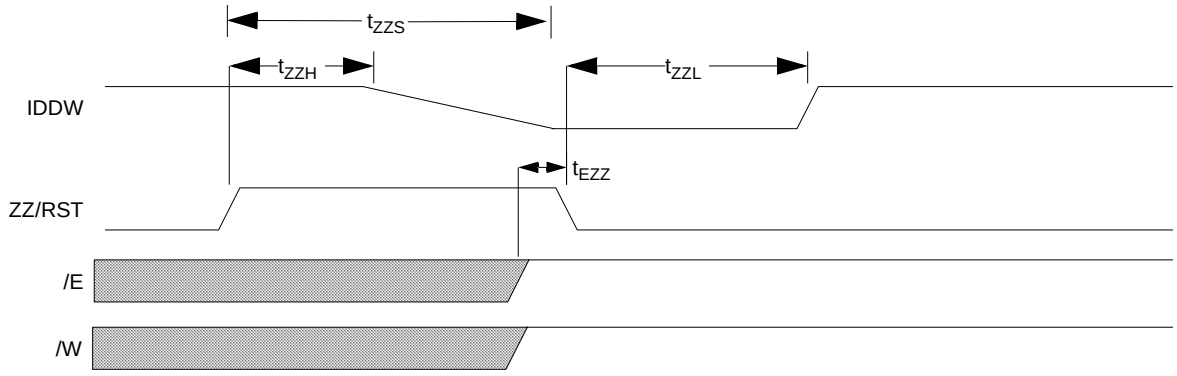
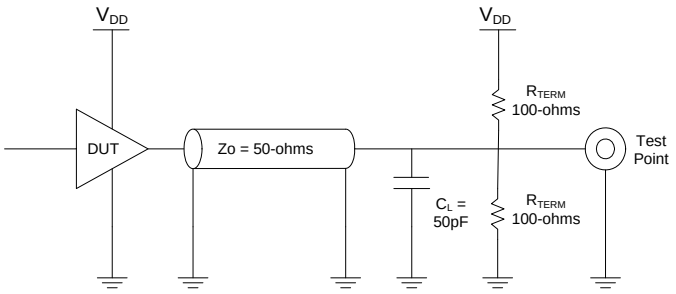


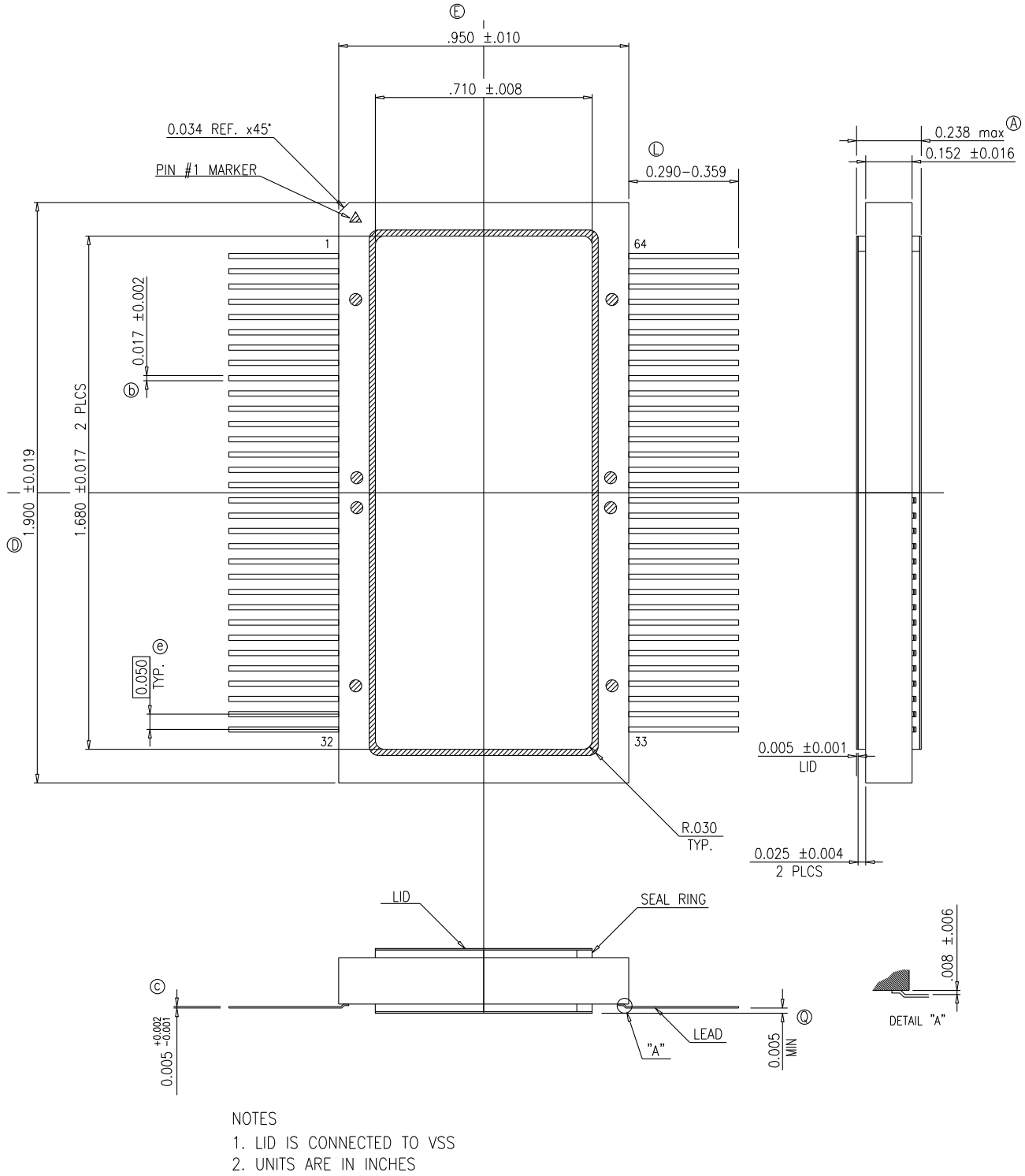
Figure 9. MRAM Sleep/Reset Mode Timing Diagram



Notes:

1. Measurement of data output occurs at the low to high or high to low transition mid-point, typically, V_{DD}/2.

Figure 10. AC Output Test Load or Equivalent

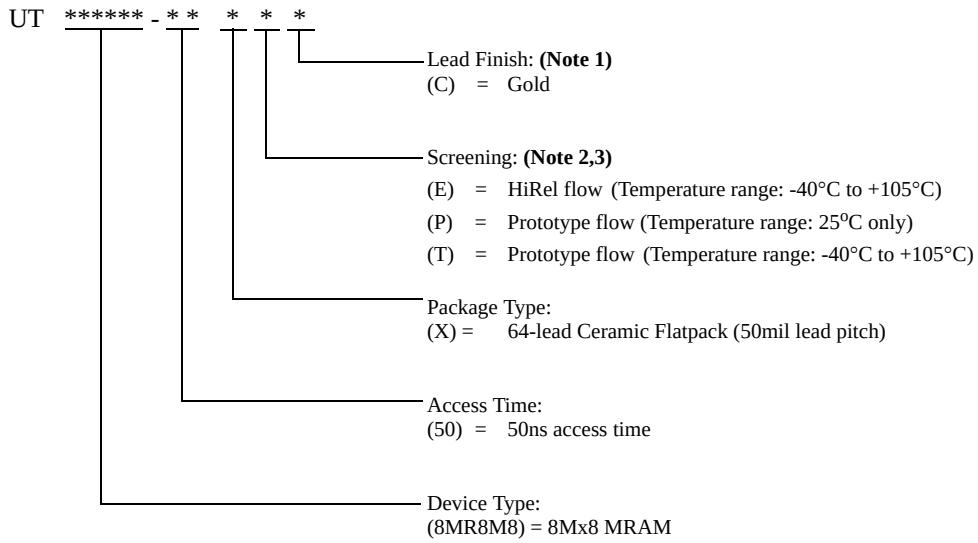


NOTES
1. LID IS CONNECTED TO VSS
2. UNITS ARE IN INCHES

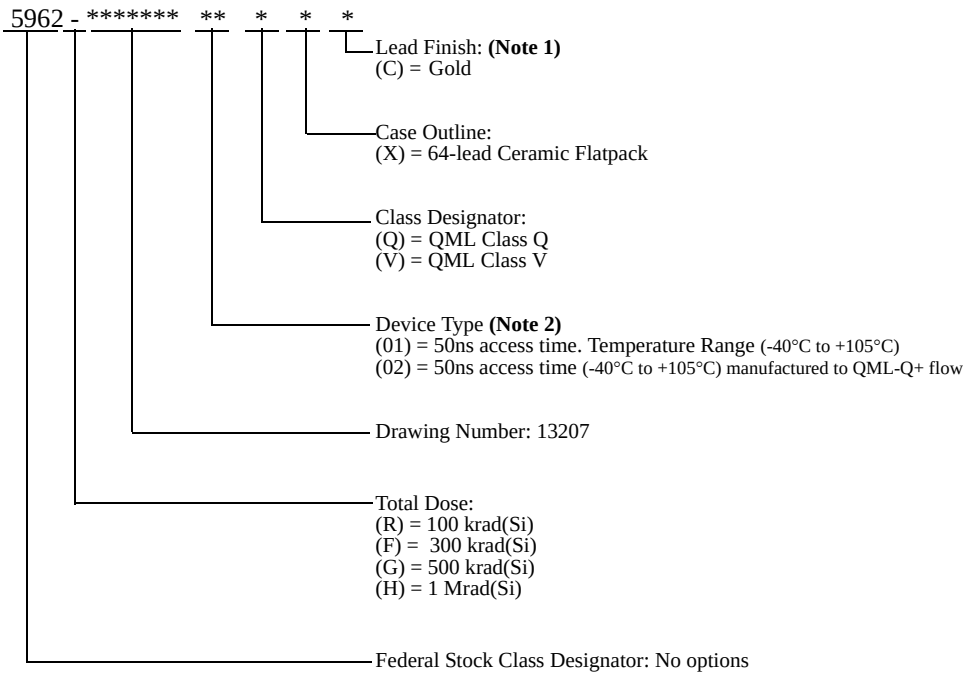
Figure 11. 64-Pin Ceramic Flatpack

ORDERING INFORMATION

8M x 8 MRAM:



Notes:
1. Lead finish is "C" (Gold) only.
2. Prototype flow per Aeroflex Colorado Springs Manufacturing Flows Document. Radiation neither tested nor guaranteed.
3. HiRel Temperature Range flow per Aeroflex Colorado Springs Manufacturing Flows Document. Radiation neither tested nor guaranteed.



Notes:

1.Lead finish is "C" (Gold) only.

2.Aeroflex's Q+ flow, as defined in Section 4.2.2d of SMD, provides QML-Q product through the SMD that is manufactured with Aeroflex's standard QML-V flow.

Cobham Colorado Springs - Datasheet Definition

Advanced Datasheet - Product In Development

Preliminary Datasheet - Shipping Prototype

Datasheet - Shipping QML & Hi-Rel

The following United States (U.S.) Department of Commerce statement shall be applicable if these commodities, technology, or software are exported from the U.S.: These commodities, technology, or software were exported from the United States in accordance with the Export Administration Regulations. Diversion contrary to U.S. law is prohibited.

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DATA SHEET REVISION HISTORY

REV	Revision Date	Description of Change	Page(s)
1.0.0	January 2016	Added new Cobham datasheet template, QML V Achieved, added ZZ/RST description of internal pull-down, updated maximum junction temperature to 150C, changed unit from uA to mA for the IINZZ specification, and added MBE Functionality verbiage and diagrams.	All