**FEATURES**

- Single 3.3-V power supply
- Fast 50ns read/write access time
- Functionally compatible with traditional asynchronous SRAMs
- Equal address and chip-enable access times
- HiRel temperature range (-40°C to +105°C)
- Automatic data protection with low-voltage inhibit circuitry to prevent writes on power loss
- CMOS and TTL compatible
- Data non-volatile for > 20 years (-40°C to +105°C)
- Read/Write endurance: Unlimited for 20 years (-40°C to +105°C)
- 64-pin ceramic flatpack package
- Operational environment:
  - Total dose: 1 Mrad(Si)
  - SEL Immune: 112 MeV·cm²/mg @125°C
  - SEU Immune: Memory Cell 112 MeV·cm²/mg @25°C
- Standard Microelectronics Drawing (SMD) - 5962-13207
  - QML Q, Q+, and V pending

**INTRODUCTION**

The Aeroflex 64Megabit Non-Volatile magnetoresistive random access memory (MRAM) is a high-performance memory multichip module (MCM) compatible with traditional asynchronous SRAM operations, organized as either four 2M words by 8 bits or one 8M words by 8 bits.

The MRAM is equipped with five chip enables (/En), a single write enable (/W), and a single output enable (/G) pins, allowing for significant system design flexibility without bus contention. Data is non-volatile for > 20 years at temperature and data is automatically protected against power loss by a low voltage write inhibit.

The 64Mb MRAM is designed specifically for operation in HiREL environments. As shown in Table 4, the magnetoresistive bit cells are immune to Single Event Effects (SEE). To guard against transient effects, an Error Correction Code (ECC) is included within the device. ECC check bits are generated and stored within the MRAM array during writes. The MBE pin identifies that ECC logic has detected two bit errors during the current read cycle.

![Figure 1. UT8MR8M8 MRAM Block Diagram](image-url)
DEVICE OPERATION

The UT8MR8M8 has control inputs called Chip Enable (/E[3:0]), Chip Enable All (/E_ALL), Write Enable (/W), Output Enable (/G), and sleep/reset mode (ZZ/RST); 23 address inputs, A[22:0]; eight bidirectional data lines, DQ[7:0]; and a Multi-bit Error Flag (MBE). /E[3:0] controls device selection, active, and standby modes. Asserting /E[3:0] enables the device, causes IDD to rise to its active value, and decodes the 21 address inputs, A[20:0], to select one of 16,777,216 words in the memory. Note: Only one Chip Enable may be active at any time. Asserting /E_ALL allows the device to be addressed as a single, 64Mb memory using address bits A21 and A22 to decode and select 1 of 4 MRAM die. /W controls read and write operation. During a read cycle, /G must be asserted to enable the outputs. ZZ/RST controls the sleep/reset mode operation and provides device reset capability. Enabling sleep/reset mode causes all other inputs to be don't cares. ZZ/RST places all die into internal low power even while system power is still applied to VDD. The MBE pin is an open drain in which when pulled down, it identifies that ECC logic has detected two bit errors during the current read cycle. It allows for wired-or of multiple MBE when using multiple MRAMs.

Table 1. 8M x 8 Pin Functions

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>A[22:0]</td>
<td>Address Input</td>
</tr>
<tr>
<td>/E[3:0]</td>
<td>Chip Enable</td>
</tr>
<tr>
<td>/E_ALL</td>
<td>Chip Enable All</td>
</tr>
<tr>
<td>/W</td>
<td>Write Enable</td>
</tr>
<tr>
<td>/G</td>
<td>Output Enable</td>
</tr>
<tr>
<td>DQ[7:0]</td>
<td>Data I/O</td>
</tr>
<tr>
<td>VDD</td>
<td>Power Supply</td>
</tr>
<tr>
<td>VSS</td>
<td>Ground</td>
</tr>
<tr>
<td>ZZ/RST</td>
<td>Deep Power Down/Reset</td>
</tr>
<tr>
<td>MBE²</td>
<td>Multi-Bit Error Flag</td>
</tr>
<tr>
<td>NUO</td>
<td>Not used output Do not connect Driven internally</td>
</tr>
</tbody>
</table>

Notes:
1. Only one /E[3:0] pin may be active at any time.
2. MBE pin is not functionally tested for prototypes.

Table 2. Chip Enable Functions Table

<table>
<thead>
<tr>
<th>/E_ALL</th>
<th>/E_0</th>
<th>/E_1</th>
<th>/E_2</th>
<th>/E_3</th>
<th>A22</th>
<th>A21</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>MRAM Die 0 Enabled</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>MRAM Die 1 Enabled</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>MRAM Die 3 Enabled</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>MRAM Die 2 Enabled</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>X</td>
<td>X</td>
<td>MRAM Die 0 Enabled</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>X</td>
<td>X</td>
<td>MRAM Die 1 Enabled</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>X</td>
<td>X</td>
<td>MRAM Die 2 Enabled</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>X</td>
<td>MRAM Die 3 Enabled</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>X</td>
<td>MRAM Die 1 Enabled</td>
</tr>
</tbody>
</table>

*Note: Only one /E[3:0] pin may be active at any time.
READ CYCLE

A combination of /W greater than VIH (min) and a single /En less than VIL (max) defines a read cycle. Read access time is measured from the latter of chip enable, output enable, or valid address to valid data output.

MRAM Read Cycle 1, the Address Access in Figure 4a, is initiated by a change in address inputs after a single /En is asserted, /G asserted and /W deasserted. Valid data appears on data outputs DQ[7:0] after the specified tAVAQV is satisfied. Outputs remain active throughout the entire cycle. As long as a single chip enable and output enable are active, the address inputs may change at a rate equal to the minimum read cycle time (tAVA).

MRAM Read Cycle 2, the Chip Enable-controlled Access in Figure 4b, is initiated by a single /En going active while /G remains asserted, /W remains deasserted, and the addresses remain stable for the entire cycle. After the specified tELOQV is satisfied, the eight-bit word addressed by A[20:0] is accessed and appears at the data outputs DQ[7:0].

WRITE CYCLE

A combination of /W and a single /En less than VIl (max) defines a write cycle. The state of /G is a “don’t care” for a write cycle. The outputs are placed in the high-impedance state when either /G is greater than VIl (min), or when /W is less than VIl (max).

Write Cycle 1, the Write Enable-controlled Access in Figure 5a, is defined by a write terminated by /W going high, with a single /En still active. The write pulse width is defined by tWLWH when the write is initiated by /W, and by tETHW when the write is initiated by a single /En. Unless the outputs have been previously placed in the high-impedance state by /G, the user must wait tWLQZ before applying data to the nine bidirectional pins DQ[7:0] to avoid bus contention.

### OPERATIONAL ENVIRONMENT

The UT8MR8M8 MRAM incorporates special design and layout features which allows operation in harsh environments.

### POWER UP AND POWER DOWN SEQUENCING

The MRAM is protected from write operations whenever VDD is less than VW. As soon as VDD exceeds VDD(min), there is a startup time of 2 ms before read or write operations can start. This time allows memory power supplies to stabilize. The /En and /W control signals should track VDD on power up to VDD - 0.2 V or VIL (whichever is lower) and remain high for the startup time. In most systems, this means that these signals should be pulled up with a resistor so the signal remains high if the driving signal is Hi-Z during power up. Any logic that drives /En and /W should hold the signals high with a power-on reset signal for longer than the startup time. During power loss or brownout where VDD goes below VW, writes are protected and a startup time must be observed when power returns above VDD(min).

The MRAM supports sleep/reset mode operation using the ZZ/RST control pin. To enter sleep mode/reset, ZZ/RST must be pulled high. The device will enter sleep/reset mode within 40ns. In order to exit sleep/reset mode, /En and /W must be high before ZZ/RST is pulled low. As soon as ZZ/RST is driven low, the user must allow 100us before performing any other operation in order for the device to properly initialize. Aeroflex recommends designing a system level method to toggle the ZZ/RST pin in order to reset the MRAM device.
Figure 4. UT8MR2M8 Power Up and Power Down Sequencing Diagram
ABSOLUTE MAXIMUM RATINGS\(^1\)
(Referenced to V\text{SS})

The device contains protection against magnetic fields. Precautions should be taken to avoid device exposure of any magnetic field intensity greater than specified.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V\text{DD}</td>
<td>Supply Voltage(^2)</td>
<td>-0.5 to 4.3</td>
<td>V</td>
</tr>
<tr>
<td>V\text{IN}</td>
<td>Voltage on any pin(^2)</td>
<td>-0.5 to V\text{DD}+0.5</td>
<td>V</td>
</tr>
<tr>
<td>I\text{IO}</td>
<td>DC I/O current per pin @ T\text{J} = 125° for 20yrs</td>
<td>± 20</td>
<td>mA</td>
</tr>
<tr>
<td>P\text{D}</td>
<td>Package power dissipation(^3)</td>
<td>4</td>
<td>W</td>
</tr>
<tr>
<td>T\text{J}</td>
<td>Maximum junction temperature</td>
<td>+125</td>
<td>°C</td>
</tr>
<tr>
<td>θ\text{JC}</td>
<td>Thermal resistance junction to case – Single Die</td>
<td>5</td>
<td>°C/W</td>
</tr>
<tr>
<td>T\text{STG}</td>
<td>Storage temperature</td>
<td>-65 to +125</td>
<td>°C</td>
</tr>
<tr>
<td>ESD\text{HBM}</td>
<td>ESD</td>
<td>&gt;2000</td>
<td>V</td>
</tr>
<tr>
<td>H\text{max_write}</td>
<td>Maximum magnetic field during write</td>
<td>8000</td>
<td>A/m</td>
</tr>
<tr>
<td>H\text{max_read}</td>
<td>Maximum magnetic field during read or standby</td>
<td>8000</td>
<td>A/m</td>
</tr>
</tbody>
</table>

Notes:
1. Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to excessive voltages or magnetic fields could affect device reliability.
2. All voltages are referenced to V\text{SS}.
3. Power dissipation capability depends on package characteristics and use environment.

RECOMMENDED OPERATING CONDITIONS

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>LIMITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>T\text{C}</td>
<td>Operating case temperature</td>
<td>-40°C to +105°C</td>
</tr>
<tr>
<td>V\text{DD}</td>
<td>Operating supply voltage</td>
<td>3.0V to 3.6V</td>
</tr>
<tr>
<td>V\text{WI}</td>
<td>Write inhibit voltage</td>
<td>2.5V to 3.0V(^1)</td>
</tr>
<tr>
<td>V\text{IH}</td>
<td>Input high voltage</td>
<td>2.2V to V\text{DD}+0.3V</td>
</tr>
<tr>
<td>V\text{IL}</td>
<td>Input low voltage</td>
<td>V\text{SS}-0.3V to 0.8V</td>
</tr>
</tbody>
</table>

Notes:
1. After power up or if V\text{DD} falls below V\text{WI}, a waiting period of 2 ms must be observed, and /En and /W must remain high for 2 ms. Memory is designed to prevent writing for all input pin conditions if V\text{DD} falls below minimum V\text{WI}.  

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**DC ELECTRICAL CHARACTERISTICS (Pre and Post-Radiation)**

VDD = 3.0V to 3.6V; Unless otherwise noted, Tc is per the temperature ordered.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITION</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$</td>
<td>High-level input voltage</td>
<td></td>
<td>2.0</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Low-level input voltage</td>
<td></td>
<td>0.8</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OL1}$</td>
<td>Low-level output voltage</td>
<td>$I_{OL} = 4mA, V_{DD} = V_{DD} (min)$</td>
<td>0.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OL2}$</td>
<td>Low-level output voltage</td>
<td>$I_{OL} = +100\mu A, V_{DD} = V_{DD} (min)$</td>
<td>$V_{SS} + 0.2$</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OH1}$</td>
<td>High-level output voltage</td>
<td>$I_{OH} = -4mA, V_{DD} = V_{DD} (min)$</td>
<td>2.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OH2}$</td>
<td>High-level output voltage</td>
<td>$I_{OH} = -100\mu A, V_{DD} = V_{DD} (min)$</td>
<td>$V_{DD} - 0.2$</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$C_{IN1}$</td>
<td>Input capacitance</td>
<td>$f = 1MHz @ 0V$</td>
<td>50</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>$C_{IO1}$</td>
<td>Bidirectional I/O capacitance</td>
<td>$f = 1MHz @ 0V$</td>
<td>60</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>$I_{IN}$</td>
<td>Input leakage current</td>
<td>$V_{IN} = V_{DD}$ and $V_{SS}$</td>
<td>-1</td>
<td>+1</td>
<td>$\mu$A</td>
</tr>
<tr>
<td>$I_{INZZ}$</td>
<td>Input leakage current ZZ/RST</td>
<td>$V_{IN} = V_{DD}$ and $V_{SS}$</td>
<td>-0.25</td>
<td>0.25</td>
<td>$\mu$A</td>
</tr>
<tr>
<td>$I_{OZ}$</td>
<td>Three-state output leakage current</td>
<td>$V_{O} = V_{DD}$ and $V_{SS}$, $V_{DD} = V_{DD} (max)$, $V_{O} = V_{DD}$ and $V_{SS}$</td>
<td>-1</td>
<td>+1</td>
<td>$\mu$A</td>
</tr>
<tr>
<td>$I_{OS2,3}$</td>
<td>Short-circuit output current</td>
<td>$V_{DD} = V_{DD} (max)$, $V_{O} = V_{DD}$, $V_{DD} = V_{DD} (max)$, $V_{O} = V_{SS}$</td>
<td>-100</td>
<td>+100</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{DDR}$</td>
<td>Active read supply current</td>
<td>Read mode $f = \text{max}$ ($I_{OUT} = 0mA; V_{DD} = \text{max}$)</td>
<td>140</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$I_{DDW}$</td>
<td>Active write supply current</td>
<td>Write mode $f = 10 MHz$ ($V_{DD} = \text{max}$)</td>
<td>140</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$Q_{IDD}$</td>
<td>Quiescent supply current</td>
<td>CMOS leakage current ($E = V_{DD}$; all other inputs equal $V_{SS}$ or $V_{DD}$; $V_{DD} = \text{max}$)</td>
<td>-40°C</td>
<td>30</td>
<td>mA</td>
</tr>
<tr>
<td>$Q_{IZZ4}$</td>
<td>Deep power down and reset supply current</td>
<td>CMOS leakage current ($E = V_{DD}$; all other inputs equal $V_{SS}$ or $V_{DD}$; $V_{DD} = \text{max}$)</td>
<td>+105°C</td>
<td>35</td>
<td>mA</td>
</tr>
</tbody>
</table>

**Notes:**

* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.
1. Measured only for initial qualification and after process or design changes that could affect input/output capacitance.
2. Supplied as a design limit but not guaranteed or tested.
3. Not more than one output may be shorted at a time for maximum duration of one second.
4. Allow 100$\mu$s to exit sleep/reset mode before performing any other operation.
AC CHARACTERISTICS READ CYCLE\(^1\) (Pre and Post-Radiation)*

\(V_{DD} = V_{DD} \text{ (min); Unless otherwise noted, } T_c \text{ is per the temperature ordered}

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(t_{AVAV})</td>
<td>Read cycle time</td>
<td>50</td>
<td>50</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{AVQV})</td>
<td>Address access time</td>
<td>50</td>
<td>50</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{ELQV})</td>
<td>Enable access time</td>
<td>50</td>
<td>50</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{GLQV})</td>
<td>Output enable access time</td>
<td>25</td>
<td>25</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{AXQX})</td>
<td>Output hold from address change</td>
<td>3</td>
<td>3</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{ELQX})</td>
<td>Enable low to output active</td>
<td>3</td>
<td>3</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{GLQX})</td>
<td>Output enable low to output active</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{EHQZ})</td>
<td>Enable high to output Hi-Z</td>
<td>0</td>
<td>15</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{GHQZ})</td>
<td>Output enable high to output Hi-Z</td>
<td>0</td>
<td>15</td>
<td>ns</td>
</tr>
</tbody>
</table>

**Notes:**

* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25\(^\circ\)C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.
1. \(/W\) is high for read cycle. Power supplies must be properly grounded and decoupled, and bus contention conditions must be minimized or eliminated during read or write cycles.
2. Address valid before or at the same time \(/En\) goes low.
3. Transition is measured at \(+/-400mV\) from the steady-state voltage.
Figure 4a. MRAM Read Cycle 1

Figure 4b. MRAM Read Cycle 2

NOTES:
Device is continuously selected (/En ≤ VIL, G ≤ VIL).

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Aeroflex Microelectronic Solutions - HiRel
AC CHARACTERISTICS /W CONTROLLED WRITE CYCLE (Pre and Post-Radiation)*  
\(V_{DD} = V_{DD} \) (min); Unless otherwise noted, \( Tc \) is per the temperature ordered.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{AVAV} )</td>
<td>Write cycle time</td>
<td>50</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{AVWL} )</td>
<td>Address set-up time</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{AVWH} )</td>
<td>Address valid to end of write (/G high)</td>
<td>28</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{AVWH} )</td>
<td>Address valid to end of write (/G low)</td>
<td>28</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{WLWH} )</td>
<td>Write pulse width (/G high or low)</td>
<td>28</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{WHDX} )</td>
<td>Data valid to end of write</td>
<td>10</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{WHDX} )</td>
<td>Data hold time</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{WLOZ} )</td>
<td>Write low to data Hi-Z</td>
<td>0</td>
<td>15</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{WHQX} )</td>
<td>Write high to output active</td>
<td>3</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{WHAX} )</td>
<td>Write recovery time</td>
<td>16</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

Notes:

* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1. All write occurs during the overlap of /En low and /W low. Power supplies must be properly grounded and decoupled, and bus contention conditions must be minimized or eliminated during read or write cycles. If /G goes low at the same time or after /W goes low, the output will remain in a high impedance state.
2. All write cycle timings are referenced from the last valid address to the first transition address.
3. Transition is measured \( +/-400 \text{mV} \) from the steady-state voltage.

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*Figure 5a. MRAM Write Cycle 1 (/W Controlled Access)*
AC CHARACTERISTICS /En CONTROLLED WRITE CYCLE¹ (Pre and Post-Radiation)*

V_{DD}= V_{DD}(min); Unless otherwise noted, Tc is per the temperature ordered.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_{AVAV}²</td>
<td>Write cycle time</td>
<td>50</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{AVEL}</td>
<td>Address set-up time</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{AVEH}</td>
<td>Address valid to end of write (/G high)</td>
<td>28</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{AVEH}</td>
<td>Address valid to end of write (/G low)</td>
<td>28</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{ELEH}</td>
<td>Enable to end of write (/G high)</td>
<td>28</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{ELWH}</td>
<td>Enable to end of write (/G low)</td>
<td>28</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{DVEH}</td>
<td>Data valid to end of write</td>
<td>10</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{EHDX}</td>
<td>Data hold time</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{EHAX}</td>
<td>Write recovery time</td>
<td>16</td>
<td></td>
<td>ns</td>
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Notes:

* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1. All write occurs during the overlap of /En low and /W low. Power supplies must be properly grounded and decoupled, and bus contention conditions must be minimized or eliminated during read or write cycles. If /G goes low at the same time or after /W goes low, the output will remain in a high impedance state.

2. All write cycle timings are referenced from the last valid address to the first transition address.

3. If /En goes low at the same time or after /W goes low, the output will remain in a high-impedance state. If /En goes high at the same time or before /W goes high, the output will remain in a high-impedance state.

4. Transition is measured +/-400mV from the steady-state voltage.

Figure 5b. MRAM Write Cycle 2 (/En Controlled)
AC CHARACTERISTICS SLEEP/RESET MODE (Pre and Post-Radiation)*

$V_{DD} = V_{DD} \text{(min)}$; Unless otherwise noted, $T_c$ is per the temperature ordered.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
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<tr>
<td>$t_{ZZL}$\textsuperscript{1,3}</td>
<td>Sleep/reset mode exit delay</td>
<td></td>
<td>100</td>
<td>$\mu$s</td>
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<tr>
<td>$t_{ZZH}$\textsuperscript{2,3}</td>
<td>Sleep/reset mode access time</td>
<td>50</td>
<td></td>
<td>ns</td>
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<tr>
<td>$t_{EZZ}$\textsuperscript{3}</td>
<td>Sleep/reset mode exit setup time</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{ZZS}$\textsuperscript{3}</td>
<td>Sleep/reset mode settle time</td>
<td>200</td>
<td></td>
<td>$\mu$s</td>
</tr>
</tbody>
</table>

Notes:
* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25ºC per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.
1. /En and /W must be high when ZZ/RST is pulled low in order to exit sleep/reset mode.
2. ZZ/RST must be high for 40ns in order to enter sleep/reset mode.
3. Parameters are supplied as a design limit, but are not tested nor guaranteed.

Figure 6. MRAM Sleep/Reset Mode Timing Diagram

Notes:
1. Measurement of data output occurs at the low to high or high to low transition mid-point, typically, $V_{DD}/2$.

Figure 7. AC Output Test Load or Equivalent
Figure 8. 64-Pin Ceramic Flatpack

NOTES
1. LID IS CONNECTED TO VSS
2. UNITS ARE IN INCHES
ORDERING INFORMATION

8M x 8 MRAM:

UT ***** _ * * * * * * * Lead Finish: (Note 1)
(C) = Gold

Screening: (Note 2,3)
(E) = HiRel flow (Temperature range: -40°C to +105°C)
(P) = Prototype flow (Temperature range: 25°C only)
(T) = Prototype flow (Temperature range: -40°C to +105°C)

Package Type:
(X) = 64-lead Ceramic Flatpack (50mil lead pitch)

Access Time:
(50) = 50ns access time

Device Type:
(8MR8M8) = 8Mx8 MRAM

Notes:
1. Lead finish is "C" (Gold) only.
8M x 8 MRAM: SMD

5962 - ******* ** * *

Lead Finish: (Note 1)
(C) = Gold

Case Outline:
(X) = 64-lead Ceramic Flatpack

Class Designator:
(Q) = QML Class Q (In development, contact factory)
(V) = QML Class V (In development, contact factory)

Device Type (Note 2)
(01) = 50ns access time. Temperature Range (-40°C to +105°C)
(02) = 50ns access time (-40°C to +105°C) manufactured to QML-Q+ flow

Drawing Number: 13207

Total Dose:
(R) = 100 krad(Si)
(F) = 300 krad(Si)
(G) = 500 krad(Si)
(H) = 1 Mrad(Si)

Federal Stock Class Designator: No options

Notes:
1. Lead finish is "C" (Gold) only.
2. Aeroflex’s Q+ flow, as defined in Section 4.2.2d of SMD, provides QML-Q product through the SMD that is manufactured with Aeroflex’s standard QML-V flow.
Our passion for performance is defined by three attributes represented by these three icons: solution-minded, performance-driven and customer-focused.
### DATA SHEET REVISION HISTORY

<table>
<thead>
<tr>
<th>Revision Date</th>
<th>Description of Change</th>
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<tr>
<td>March 2015</td>
<td>Initial Release of Datasheet</td>
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36-00-01-000
Ver. 1.0.0

Aeroflex Microelectronic Solutions - HiRel