Standard Products

UT8MR8M8-EVB 64Megabit Non-Volatile MRAM Evaluation Board

User Manual
July 2012
www.aeroflex.com/memories

1.0 INTRODUCTION

The Aeroflex 64Megabit Non-Volatile magnetoresistive random access memory (MRAM) is a high-performance memory multichip module (MCM) compatible with traditional asynchronous SRAM operations, organized as four individual 16,777,216 words by 8 bits. The MRAM is equipped with five chip enables (/En), a single write enable (/W), and a single output enable (/G) pin, allowing for significant system design flexibility without bus contention. Data is non-volatile for > 15 years at temperature and data is automatically protected against power loss by a low voltage write inhibit.

The UT8MR8M8-EVB allows the user access to most all the features of the 64Mb MRAM via bench top evaluation or using the UT699 LEON-3FT evaluation board.

2.0 SCOPE

This document describes the features and necessary steps to set-up and operate the Aeroflex Colorado Springs 64Megabit Non-Volatile MRAM Evaluation Board. Users must be familiar with the UT699 LEON-3FT Processor and the 64Megabit Non-Volatile MRAM datasheets.

3.0 REFERENCE DOCUMENTS

Aeroflex Colorado Springs, "UT8MR8M8 64Megabit Non-Volatile MRAM" Datasheet,
www.aeroflex.com/memories

Aeroflex Gaisler "GR-CPCI-UT699 LEON3-FT CPCI Development Board" User Manual,
www.aeroflex.com/LEON

Aeroflex Colorado Springs, "UT699 32-bit Fault Tolerant SPARC^{TM} V8/LEON3FT Processor" Datasheet,
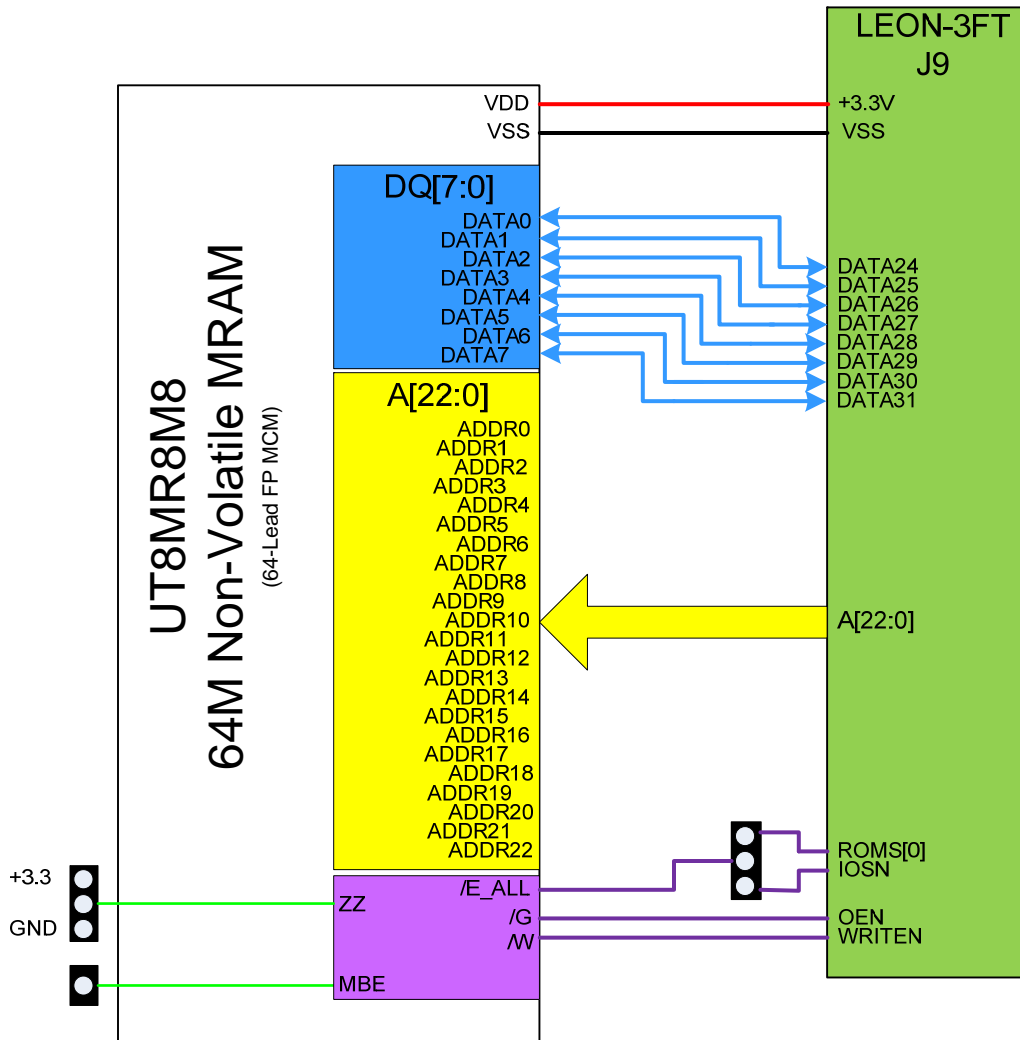www.aeroflex.com/LEON

4.0 FUNCTIONAL DIAGRAM

Figure 1. Notional UT8MR8M8-EVB block diagram

5.0 FEATURES AND GENERAL OPERATION

The Aeroflex 64Megabit Non-Volatile MRAM Evaluation Board provides the user with a flexible means to configure, control, access, and read/write data to the UT8MR8M8 device. Power to the board may be provided through the J9 connector on the GR-UT699 CPCI Development Board or through the 100 mil connector J8 on the UT8MR8M8-EVB. Only one power source should be used at a time.

5.1 Power

5.1.1   External Power

Power to the UT8MR8M8-EVB may be provided externally using 3.3V if using in a bench top only configuration.
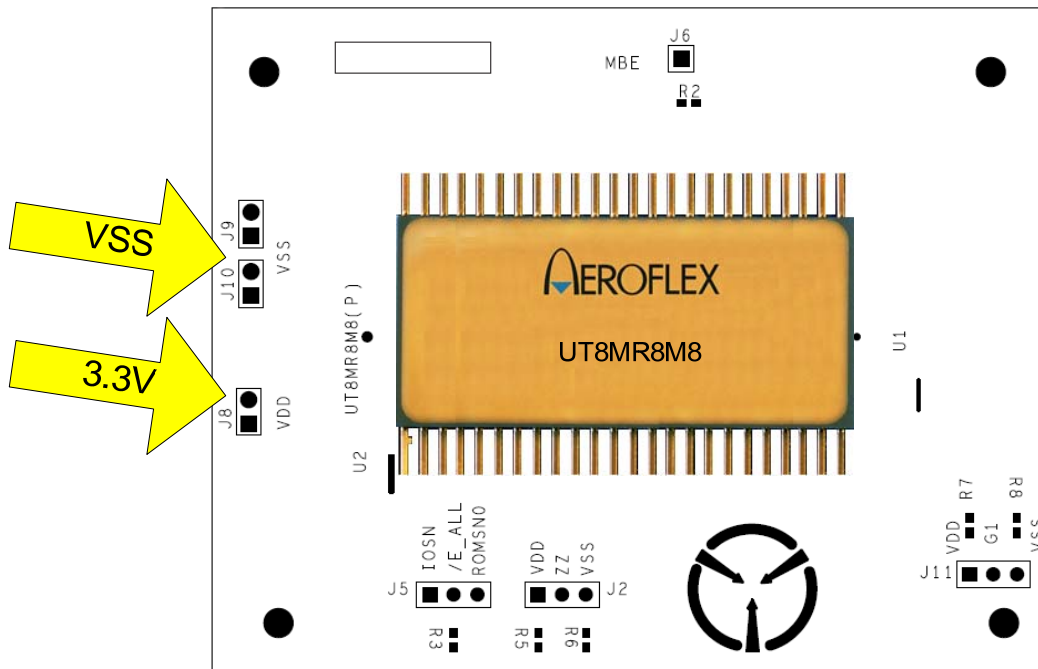

Figure 2. External Power Jumper Configuration Settings

5.1.2 Aeroflex Gaisler Board Power

Power to the UT8MR8M8-EVB is also provided from the J9 connector on the GR-CPCI-UT699 LEON3-FT CPCI Development Board. J7, the 120 pin connector, is located on the back side of the EVB.

Use caution when mating the 64Megabit Non-Volatile MRAM Evaluation Board to the LEON-3FT evaluation board. Ensure that the mating connectors are lined up and that the power is removed from the GR-cPCI-UT699 eval board prior to plugging in the MRAM evaluation board.

Table 1. LEON-3FT-EVB Power Pins (J9)

LEON-3FT connector	
Pin	Signal
10	3.3V
20	3.3V
30	3.3V
40	3.3V
51	3.3V
71	3.3V
81	3.3V
91	3.3V
101	3.3V
111	3.3V

Table 2. LEON-3FT-EVB Ground pins (J9)

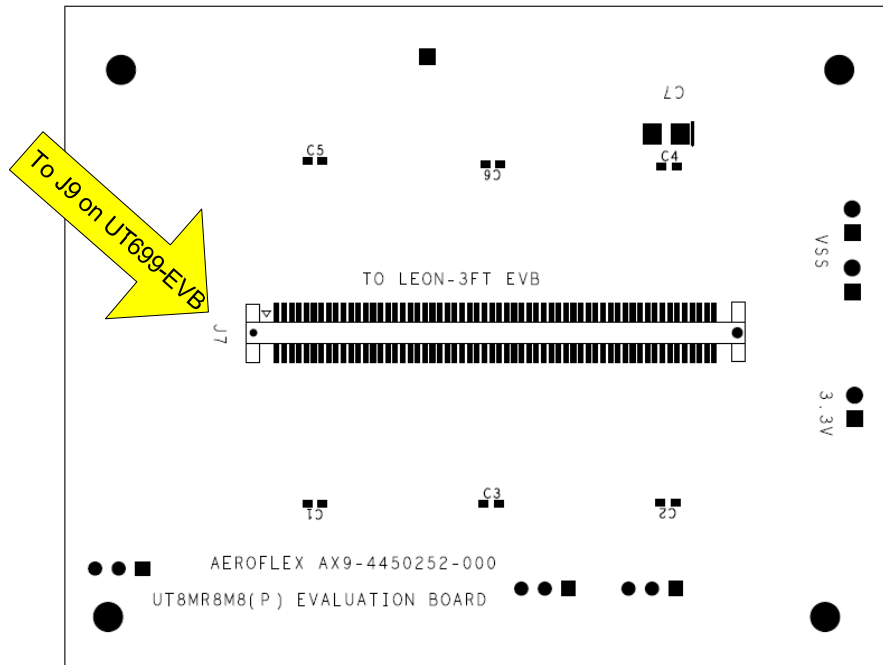| LEON-3FT connector	
Pin	Signal
1	VSS
3	VSS
5	VSS
7	VSS
11	VSS
21	VSS
31	VSS
41	VSS
50	VSS
60	VSS
61	VSS
70	VSS
80	VSS
90	VSS
100	VSS
110	VSS
114	VSS
116	VSS
118	VSS
120	VSS

Figure 3. Aeroflex Gaisler LEON-3FT J7 to J9 connector

5.2 Address Inputs

Table 3. Address Inputs J7 pin out

LEON-3FT connector (J9)		UT8MR8M8 Device (J7)	
Pin	Signal	Pin	Signal
45	A0	10	A0
76	A1	9	A1
44	A2	8	A2
77	A3	7	A3
43	A4	6	A4
78	A5	28	A5
42	A6	27	A6
79	A7	26	A7
39	A8	25	A8
82	A9	24	A9
38	A10	41	A10
83	A11	40	A11
37	A12	39	A12
84	A13	38	A13
36	A14	37	A14
85	A15	58	A15
35	A16	57	A16
86	A17	56	A17
34	A18	55	A18
87	A19	11	A19
33	A20	59	A20
88	A21	22	A21
32	A22	23	A22

5.3 Data I/O

The UT8MR8M8 has eight bidirectional data lines, DQ[7:0]. The data inputs/outputs are connected to J7 as shown in table 4.

Table 4. Data I/O J7 pin out

LEON-3FT connector (J9)		UT8MR8M8 Device (J7)	
Pin	Signal	Pin	Signal
95	D24	46	DATA0
97	D25	47	DATA1
99	D26	50	DATA2
103	D27	51	DATA3
105	D28	14	DATA4
107	D29	15	DATA5
109	D30	18	DATA6
113	D31	19	DATA7

5.4 Chip Enable

Asserting /E_All allows the device to be addressed as a single, 64Mb memory using address bits A21 and A22 to decode and select 1 of 4 MRAM die.

Table 5. Enable Signals LEON-3FT (J5)

LEON-3FT connector (J9)		UT8MR8M8 Device (J7)	
Pin	Signal	Pin	Signal
48	ROMSN0	21	Can be jumpered to /E_ALL for LEON-3FT to control the UT8MR8M8
74	IOSN	21	Can be jumpered to /E_ALL

The user can exercise either the IOSN or ROMSN0 pin on the LEON-3FT to exercise the /E_All pin on the MRAM. There is a three pin header, J5, that allows the user to select IOSN or ROMSN0 to control the /E_All pin.
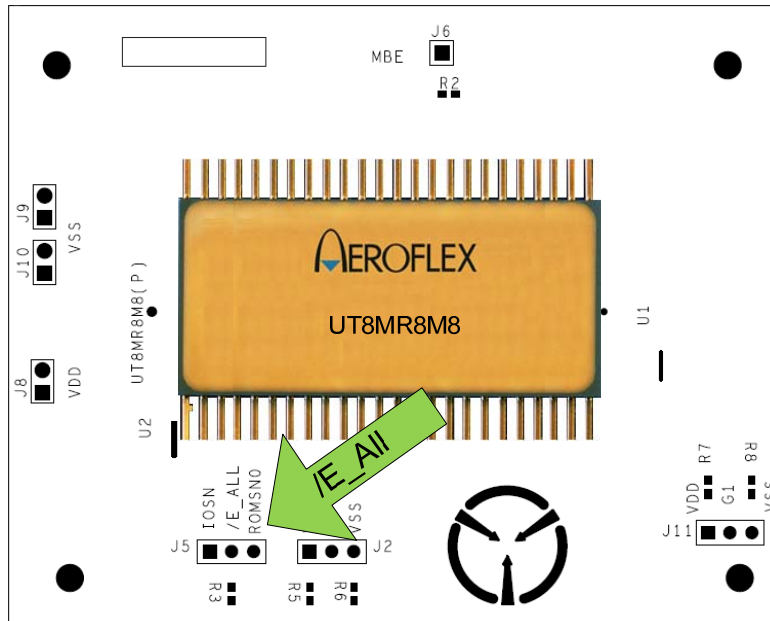

Figure 6. /E_All header control

5.4.1 Use as an External Memory with LEON
Set J5 to ROMSN0 on the UT8MR8M8-EVB and uninstall JP6 on the UT699-EVB.

5.4.2 Use as IO Space
Set J5 to IOSN option on the UT8MR8M8-EVB and install JP6 on the UT699-EVB.

5.5 Write Enable (/W)

/W controls read and write operation. During a read cycle, /G must be asserted to enable the outputs.

Table 6. Write Enable LEON-3FT J7 to J9 connector

LEON-3FT connector (J9)		UT8MR8M8 Device (J7)	
Pin	Signal	Pin	Signal
46	WEB	42	/W

5.6 Output Enable (/G)

/W controls read and write operation. During a read cycle, /G must be asserted to enable the outputs.

Table 7. Output Enable LEON-3FT J7 to J9 connector

LEON-3FT connector (J9)		UT8MR8M8 Device (J7)	
Pin	Signal	Pin	Signal
47	OEB	53	/G

5.7 Deep Sleep Power Down (ZZ)

ZZ controls the sleep mode operation. Enabling sleep mode causes all other inputs to be do not cares. ZZ places all die into internal low power even while system power is still applied to VDD. Pin 12 on the UT8MR8M8 are routed to a three pin header J2. The center pin on the three pin J2 header is tied to the ZZ pin, the other pins are tied to VDD and VSS. Please refer to the UT8MR8M8 datasheet for further information.
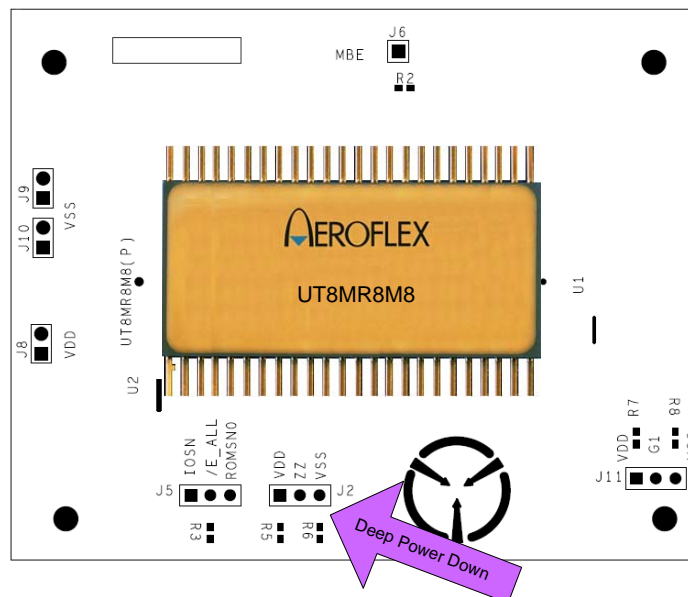

Figure 7. ZZ pin

5.8 Multi-Bit Error Flag (MBE)

The open drain MBE pin drives low when ECC logic detects two bit errors during the current read cycle. It allows for wired-or of multiple MBE signals when using multiple MRAMs. The MBE signal is routed to the one pin J6 header. This pin can be monitored if the user chooses to do so.
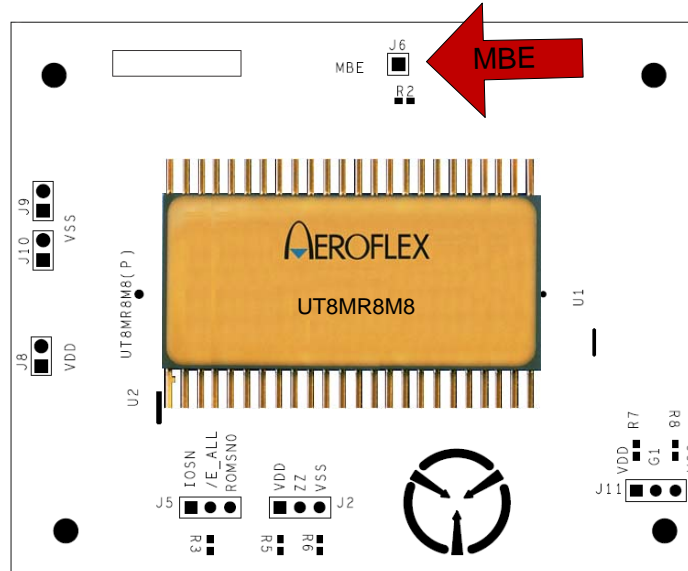

Figure 8. MBE pin

6.0 Quick Start Guide

The following steps describe how the user to get the UT8MR8M8-EVB up and running with the UT699 LEON-3FT EVB.

1. Connect J5to the UT8MR8M8-EVB to ROMSN0 for using MRAM as PROM
   - or -
   Connect J5to the UT8MR8M8-EVB to IOSN for using MRAM as IO Space

2. Disconnect power to the UT699-EVB
3. Plug the UT8MR8M8-EVB J7 to J9 on the UT699-EVB
4. Configure DIP switches S3 and S4 as shown in Table 9 and 10.
5. Reference Section 3 "SETTING UP AND USING THE BOARD" in the user's manual for the GR-UT699 board. Install the jumpers as indicated in Table 11.

Table 8. Quick Start LEON-3FT S3 8-bit mode Configuration

DIP Switch S3			
Switch	Function	Value	Comment
1	PIO0	0	8-bit Mode (Closed)
2	PIO1	0	8-bit Mode (Closed)
3	PIO2	0	PROM EDAC disabled (Closed)
4	PIO3	1	(Open)
5	PIO4	1	(Open)
6	PIO5	1	(Open)
7	PIO6	1	(Open)
8	PIO7	1	(Open)

Table 9. Quick Start LEON-3FT S4 Configuration

DIP Switch S4			
Switch	Function	Value	Comment
1	PIO8	1	(Open)
2	PIO9	1	(Open)
3	PIO10	1	(Open)
4	PIO11	1	(Open)
5	PIO12	1	(Open)
6	PIO13	1	(Open)
7	PIO14	1	(Open)
8	PIO15	1	(Open)

Table 10. Quick Start LEON-3FT Jumper settings for ROMSN0 or IOSN

Jumper	Jumper Setting	Comment
JP1	1-2: Do Not Install 3-4: Do Not Install 5-6: Do Not Install 7-8: Do Not Install	ASIC TEST mode pin not enabled DSU is enabled JTAG interface is enabled. Watchdog output can cause board reset
JP2	Do Not Install	Ethernet MDIO interface interrupt is not connected to GPIO4
JP3	1-3: Install	End-stub termination enabled – see section 2.4.1
JP4	1-3: Install	End-stub termination enabled – see section 2.4.1
JP5	1-2: Install 3-4: Install 5-6: Install 7-8: Install	Connects RAMSN0 and RAMSN1 to on board SRAM banks
JP6	Do Not Install 1-2: Install	Connects ROMSN0 to on board MRAM on UT8MR8M8-EVB Connects IOSN to on board MRAM on UT8MR8M8-EVB
JP7	1-2: Install 3-4: Install	PCI Host Mode clocks to backplane – see section 2.11
JP8	1-2: Install 3-4: Install 5-6: Install 7-8: Install 9-10: Install 11-12: Install 13-14: Install 15-16: Install 17-18: Install 19-20: Install	PCI Host Mode- Pull ups enabled – see section 2.11
JP9	1-2: Install 3-4: Install	PCI Host Mode – see section 2.11
JP10	1-2: Install 3-4: Install	PCI Host Mode – see section 2.11
JP11	Install	Connects to Front Panel LED indicators
JP12	1-2: Install	See section 2.9
JP13	1-2: Install	See section 2.9
JP14	Install	Can be used as current measure point for Vcore supply to ASIC
JP15	Install	Can be used as current measure point for 3.3V supply to ASIC
JP16	Install	Connected to Front Panel push buttons for RESET and BREAK
JP17	1-2: Install	Main Processor Clock is also source for SPW_CLK
JP18	1-2: Install	Board RESETN also generated PCI_RSTN for PCI Host

6. Power on the UT699-EVB
7. Using GRMON:
    a. MRAM as PROM: The following commands need to be run to set up memory configuration register 1 to allow reading and writing the MRAM when it is configured as the PROM for the UT699.
        i. `wmem 0x80000000 0x1803c811`
        ii. `mcfg1 0x1803c811`
        iii. User code

b. MRAM as I/O space: The following commands need to be run to set up memory configuration register 1 to allow reading and writing the MRAM when it is configured as I/O space for the UT699.
    i. `wmem 0x80000000 0x001BC811`
    ii. `mcfg1 0x001BC811`
    iii. User code

7.0 COMPATIBILITY WITH GR-UT699 EVALUATION BOARD

The UT8MR8M8-EVB can plug directly into the J9 connector on the LEON-3FT evaluation board. J9 on the GR-UT699 evaluation board is pinned out as listed in table 12 below.

For further information on interfacing the UT8MR8M8-EVB with the GR-UT699 Evaluation board please see the Aeroflex Gaisler GR-UT699 Development Board User Manual.

Table 11. UT8MR8M8-EVB to UT699-3FT LEON connections

LEON-3FT connector		UT8MR8M8 Device	
Pin	Signal	Pin	Signal
1			VSS
2	+5V		NC
3			VSS
4	-12V		NC
5			VSS
6	+12V		NC
7			VSS
8	D15		NC
9	D7		NC
10			3.3V
11			VSS
12	D14		NC
13	D6		NC
14	D13		NC
15	D5		NC
16	D12		NC
17	D4		NC
18	D11		NC
19	D3		NC
20			3.3V
21			VSS
22	D10		NC
23	D2		NC
24	D9		NC
25	D1		NC

26	D8		NC
27	D0		NC
28	A26		NC
29	A14		NC
30			3.3V
31			VSS
32	A22	23	A22
33	A20	59	A20
34	A18	55	A18
35	A16	57	A16
36	A14	37	A14
37	A12	39	A12
38	A10	41	A10
39	A8	25	A8
40			3.3V
41			VSS
42	A6	27	A6
43	A4	6	A4
44	A2	8	A2
45	A0	10	A0
46	WEB	42	WEB
47	OEB	53	OEB
48	ROMSN0		ROMSN0
49	RAMSN4		NC
50			VSS
51			3.3V
52	RAMSN3		NC
53	RAMSN2		NC
54	RAMSN1		NC
55	RAMSN0		NC
56	RWEN2		NC
57	RWEN0		NC
58	BRDYN		NC
59	RESETN		NC
60			VSS
61			VSS
62	CLK		NC
63	BEXCN		NC
64	RWEN1		NC
65	RWEN3		NC
66	RAMOEN0		NC
67	RAMOEN1		NC
68	RAMOEN2		NC
69	RAMOEN3		NC
70			VSS

71			3.3V
72	RAMOEN4		NC
73	RAMSN1		NC
74			IOSN
75	READ		NC
76	A1	9	A1
77	A3	7	A3
78	A5	28	A5
79	A7	26	A7
80			VSS
81			3.3V
82	A9	24	A9
83	A11	40	A11
84	A13	38	A13
85	A15	58	A15
86	A17	56	A17
87	A19	11	A19
88	A21	22	A21
89	A23		NC
90			VSS
91			3.3V
92	A25		NC
93	A27		NC
94	D16		NC
95	D24	46	DATA0
96	D17		NC
97	D25	47	DATA1
98	D18		NC
99	D26	50	DATA2
100			VSS
101			3.3V
102	D19		NC
103	D27	51	DATA3
104	D20		NC
105	D28	14	DATA4
106	D21		NC
107	D29	15	DATA5
108	D22		NC
109	D30	18	DATA6
110			VSS
111			3.3V
112	D23		NC
113	D31	19	DATA7
114			VSS
115	+12V		NC

116			VSS
117	-12V		NC
118			VSS
119	+5V		NC
120			VSS

8.0 BOARD SCHEMATICS

The schematics are for reference ONLY.

Change Block

1 MQ11
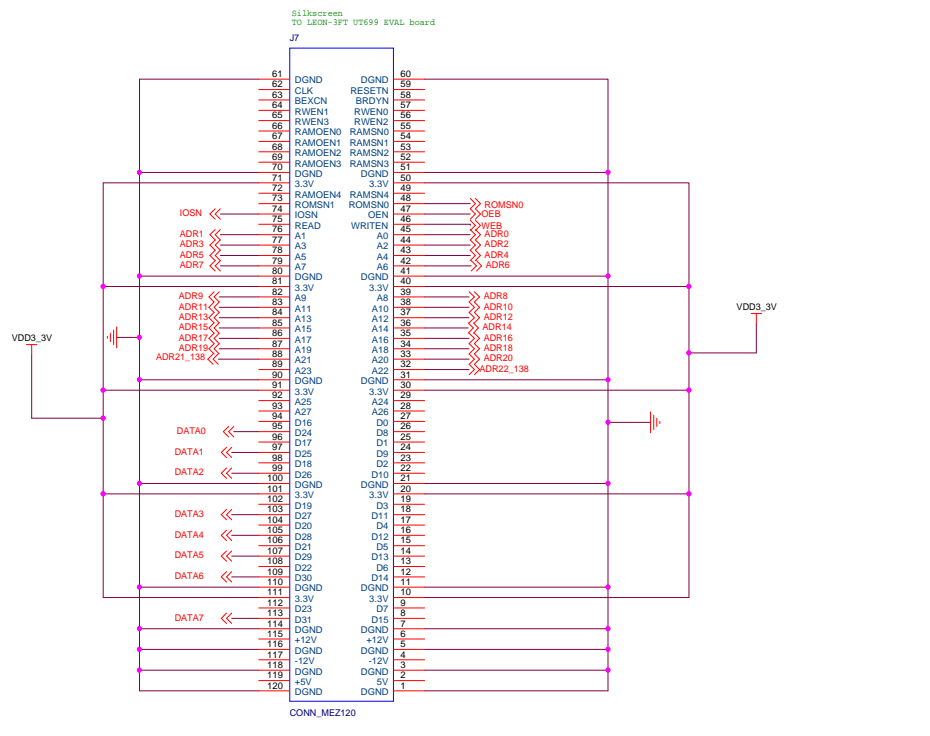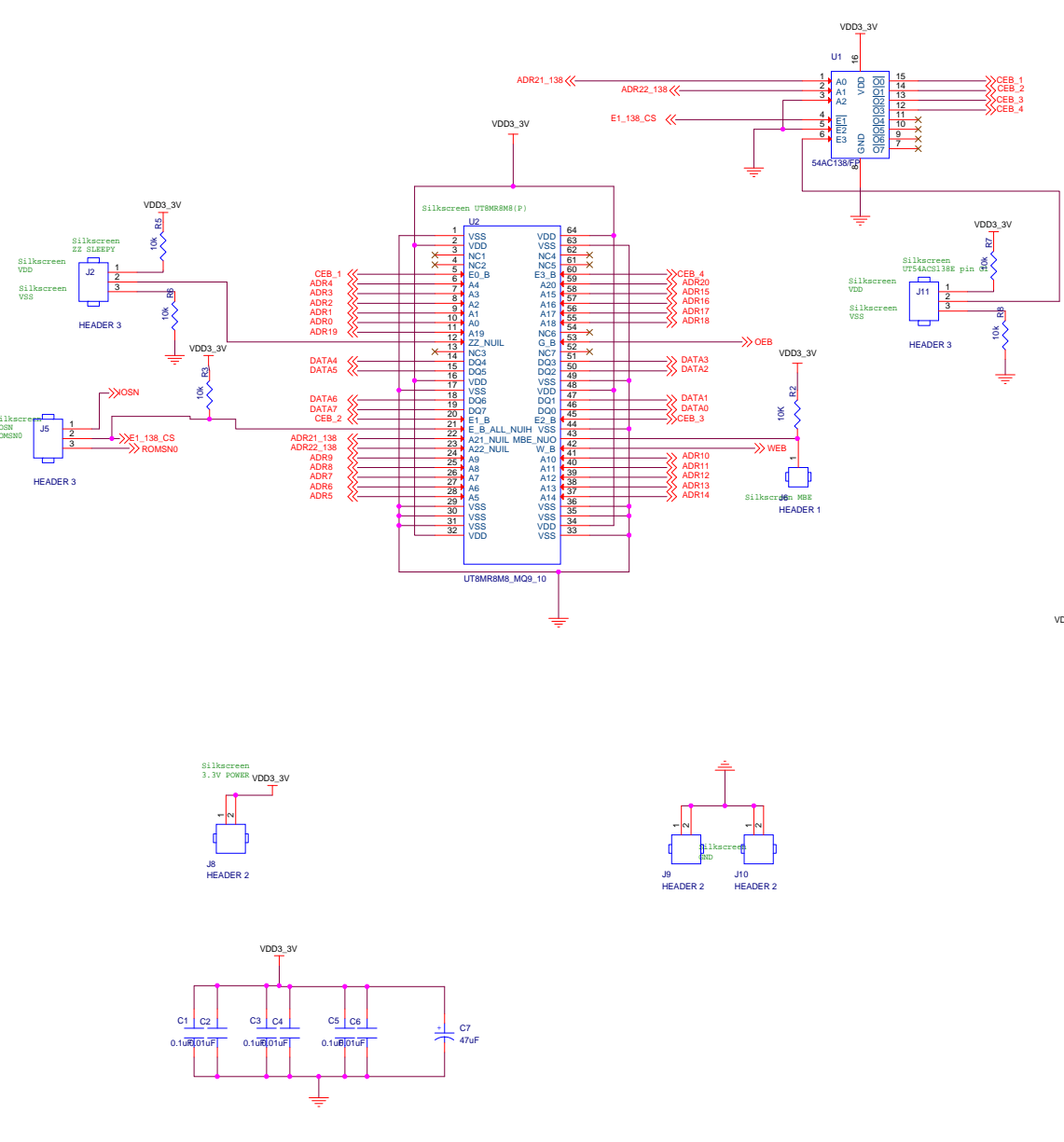
64M MRAM EVALUATION BOARD

Size	CAGE Code	DWG NO	Rev
C	65342	4350252-000	-

Tuesday, March 20, 2012

Scale

Larsen

ORDERING INFORMATION

UT *****

Device Type:
8MR8M8-EVB = 64Megabit Non-Volatile MRAM Evaluation Board

Aeroflex Colorado Springs - Datasheet Definition

Advanced Datasheet - Product In Development

Preliminary Datasheet - Shipping Prototype

Datasheet - Shipping QML & Reduced Hi – Rel