

# UT8ER1M32 32Megabit SRAM MCM

## UT8ER2M32 64Megabit SRAM MCM

### UT8ER4M32 128Megabit SRAM MCM

Data Sheet

December 2015

The most important thing we build is trust

#### FEATURES

- ❑ 20ns Read, 10ns Write maximum access times available
- ❑ Functionally compatible with traditional 1M, 2M and 4M x 32 SRAM devices
- ❑ CMOS compatible input and output levels, three-state bidirectional data bus
  - I/O Voltages 2.3V to 3.6V, 1.7V to 2.0V<sub>core</sub>
- ❑ Available densities:
  - UT8ER1M32: 33, 554, 432 bits
  - UT8ER2M32: 67, 108, 864 bits
  - UT8ER4M32: 134, 217, 728 bits
- ❑ Operational environment:
  - Total-dose: 100 krad(Si)
  - SEL Immune:  $\leq 110$  MeV-cm<sup>2</sup>/mg
  - SEU error rate =  $8.1 \times 10^{-16}$  errors/bit-day assuming geosynchronous orbit, Adam's 90% worst environment, and 6600ns default Scrub Rate Period (=97% SRAM availability)
- ❑ Packaging option:
  - 132-lead side-brazed dual cavity ceramic quad flatpack
- ❑ Standard Microelectronics Drawing:
  - UT8ER1M32: 5962-10202
    - QML Q, Q+ and Vcompliant
  - UT8ER2M32: 5962-10203
    - QML Q, Q+, and Vcompliant
  - UT8ER4M32: 5962-10204
    - QML Q and Q+ compliant

The UT8ER1M32, UT8ER2M32, and UT8ER4M32 are high performance CMOS static RAM multichip modules (MCMs) organized as two, four or eight individual 524,288 words x 32 bits dice respectively. Easy memory expansion is provided by active LOW chip enables ( $\overline{E_n}$ ), an active LOW output enable ( $\overline{G}$ ), and three-state drivers. This device has a power-down feature that reduces power consumption by more than 90% when deselected. Autonomous (master) and demanded (slave) scrubbing continues while deselected.

Writing to the device is accomplished by driving one of the chip enable ( $\overline{E_n}$ ) inputs LOW and the write enable ( $\overline{W}$ ) input LOW. Data on the 32 I/O pins (DQ0 through DQ31) is then written into the location specified on the address pins (A0 through A18). Reading from the device is accomplished by driving one of the chip enables ( $\overline{E_n}$ ) and output enable ( $\overline{G}$ ) LOW while driving write enable ( $\overline{W}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins. **Note:** Only one  $\overline{E_n}$  pin may be active at any time.

The 32 input/output pins (DQ0 through DQ31) are placed in a high impedance state when the device is deselected ( $\overline{E_n}$  HIGH), the outputs are disabled ( $\overline{G}$  HIGH), or during a write operation ( $\overline{E_n}$  LOW,  $\overline{W}$  LOW).

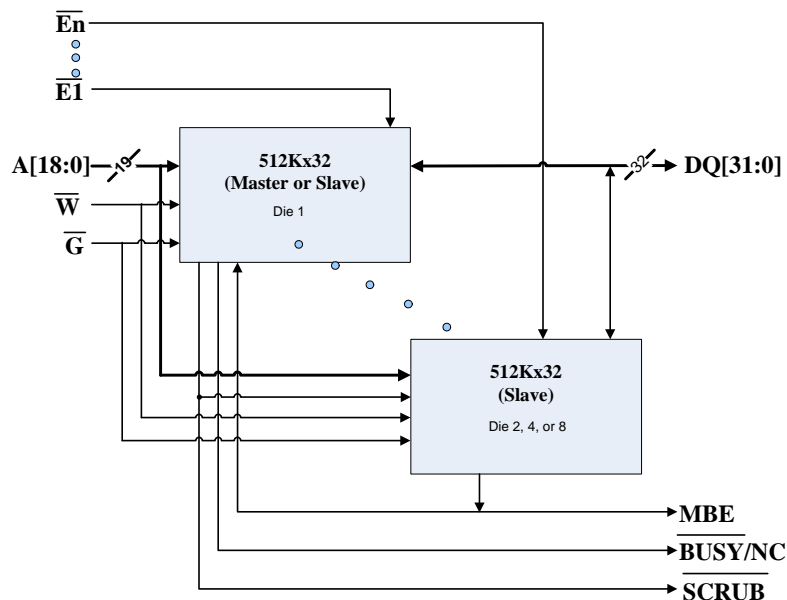
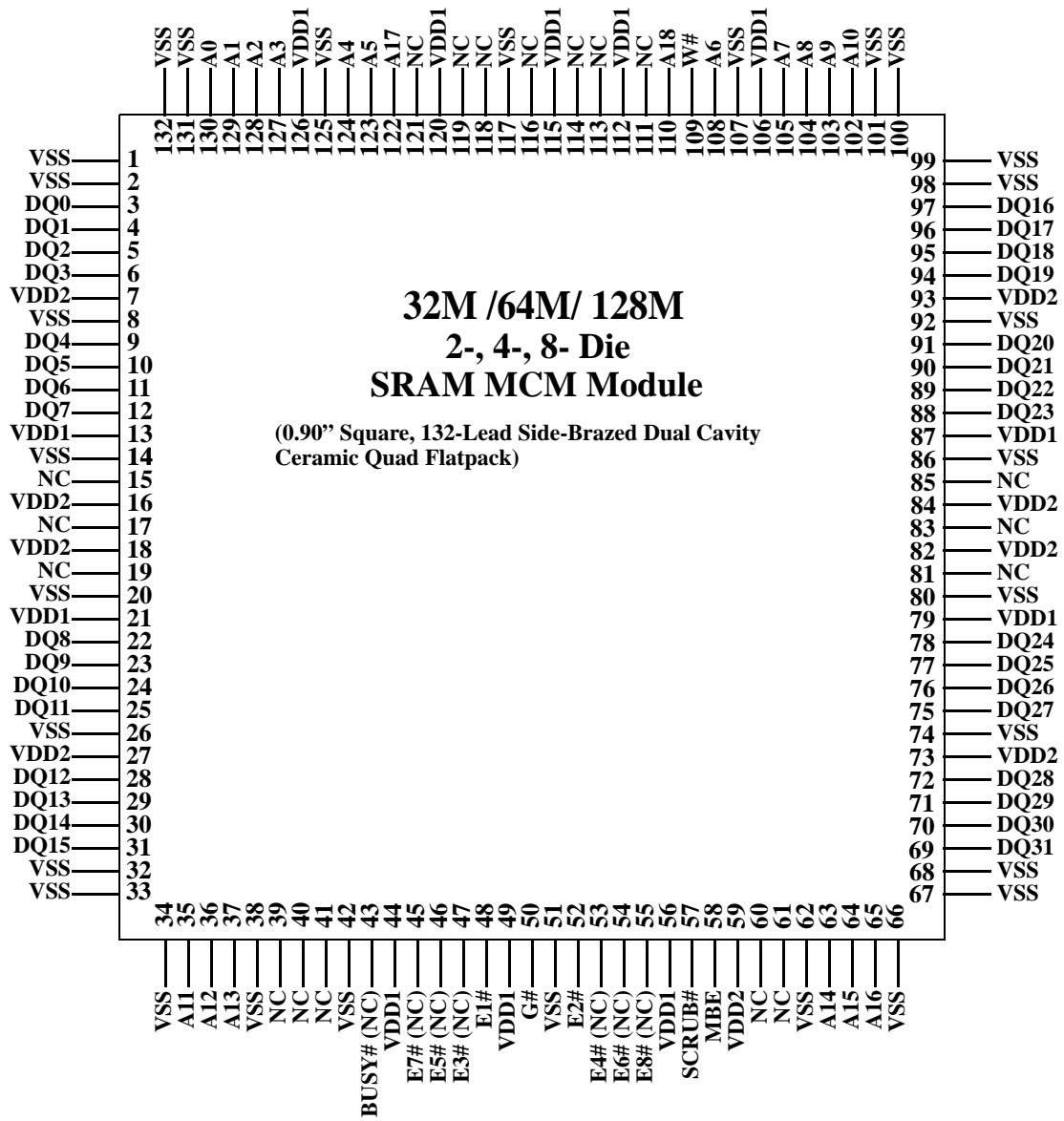


Figure 1. Block Diagram

#### INTRODUCTION



**Notes:**

1. NC = Pins are not connected on die.
2. (NC) = Depending on device option, pin may be either signal as named or NC (see Table 1).

**Figure 2. Pin Diagram**

**Table 1. Pin Description**

<b>Pin</b>	<b>Type</b>	<b>Description</b>
A(18:0)	I	Address Input
DQ(31:0)	BI	Data Input/Output
En#*	I	Enable (Active Low)
W#	I	Write Enable (Active Low)
G#	I	Output Enable (Active Low)
VDD1	P	Power (1.8V nominal)
VDD2	P	Power (3.3V nominal)
VSS	P	Ground
MBE	BI	Multiple Bit Error
SCRUB#	I	Slave SCRUB Input (Active Low)
SCRUB#	O	Master SCRUB Output
BUSY#	NC	Slave No Connect
BUSY#	O	Master Wait State Control

**Notes:**

\* n represents any number of individual MCM (multichip module) die enables. May be 1-8 depending on device option.

**Table 2. Device Option: Signal and Pin Description**

<b>Pkg Pin #</b>	<b>UT8ER1M32M (Master) Signal Name</b>	<b>UT8ER1M32S (Slave) Signal Name</b>	<b>UT8ER2M32M (Master) Signal Name</b>	<b>UT8ER2M32S (Slave) Signal Name</b>	<b>UT8ER4M32M (Master) Signal Name</b>	<b>UT8ER4M32S (Slave) Signal Name</b>	<b>Device Pin Description</b>
1	VSS	VSS	VSS	VSS	VSS	VSS	PWR
2	VSS	VSS	VSS	VSS	VSS	VSS	PWR
3	DQ0	DQ0	DQ0	DQ0	DQ0	DQ0	DATA I/O
4	DQ1	DQ1	DQ1	DQ1	DQ1	DQ1	DATA I/O
5	DQ2	DQ2	DQ2	DQ2	DQ2	DQ2	DATA I/O
6	DQ3	DQ3	DQ3	DQ3	DQ3	DQ3	DATA I/O
7	VDD2	VDD2	VDD2	VDD2	VDD2	VDD2	PWR
8	VSS	VSS	VSS	VSS	VSS	VSS	PWR
9	DQ4	DQ4	DQ4	DQ4	DQ4	DQ4	DATA I/O
10	DQ5	DQ5	DQ5	DQ5	DQ5	DQ5	DATA I/O
11	DQ6	DQ6	DQ6	DQ6	DQ6	DQ6	DATA I/O
12	DQ7	DQ7	DQ7	DQ7	DQ7	DQ7	DATA I/O
13	VDD1	VDD1	VDD1	VDD1	VDD1	VDD1	PWR
14	VSS	VSS	VSS	VSS	VSS	VSS	PWR
15	NC	NC	NC	NC	NC	NC	NC
16	VDD2	VDD2	VDD2	VDD2	VDD2	VDD2	PWR
17	NC	NC	NC	NC	NC	NC	NC
18	VDD2	VDD2	VDD2	VDD2	VDD2	VDD2	PWR
19	NC	NC	NC	NC	NC	NC	NC
20	VSS	VSS	VSS	VSS	VSS	VSS	PWR
21	VDD1	VDD1	VDD1	VDD1	VDD1	VDD1	PWR
22	DQ8	DQ8	DQ8	DQ8	DQ8	DQ8	DATA I/O
23	DQ9	DQ9	DQ9	DQ9	DQ9	DQ9	DATA I/O
24	DQ10	DQ10	DQ10	DQ10	DQ10	DQ10	DATA I/O
25	DQ11	DQ11	DQ11	DQ11	DQ11	DQ11	DATA I/O
26	VSS	VSS	VSS	VSS	VSS	VSS	PWR
27	VDD2	VDD2	VDD2	VDD2	VDD2	VDD2	PWR
28	DQ12	DQ12	DQ12	DQ12	DQ12	DQ12	DATA I/O
29	DQ13	DQ13	DQ13	DQ13	DQ13	DQ13	DATA I/O
30	DQ14	DQ14	DQ14	DQ14	DQ14	DQ14	DATA I/O

Table 2. Device Option: Signal and Pin Description

Pkg Pin #	UT8ER1M32M (Master) Signal Name	UT8ER1M32S (Slave) Signal Name	UT8ER2M32M (Master) Signal Name	UT8ER2M32S (Slave) Signal Name	UT8ER4M32M (Master) Signal Name	UT8ER4M32S (Slave) Signal Name	Device Pin Description
31	DQ15	DQ15	DQ15	DQ15	DQ15	DQ15	DATA I/O
32	VSS	VSS	VSS	VSS	VSS	VSS	PWR
33	VSS	VSS	VSS	VSS	VSS	VSS	PWR
34	VSS	VSS	VSS	VSS	VSS	VSS	PWR
35	A11	A11	A11	A11	A11	A11	ADDRESS INPUT
36	A12	A12	A12	A12	A12	A12	ADDRESS INPUT
37	A13	A13	A13	A13	A13	A13	ADDRESS INPUT
38	VSS	VSS	VSS	VSS	VSS	VSS	PWR
39	NC	NC	NC	NC	NC	NC	NC
40	NC	NC	NC	NC	NC	NC	NC
41	NC	NC	NC	NC	NC	NC	NC
42	VSS	VSS	VSS	VSS	VSS	VSS	PWR
43	BUSY#	NC	BUSY#	NC	BUSY#	NC	OUTPUT <sup>1</sup>
44	VDD1	VDD1	VDD1	VDD1	VDD1	VDD1	PWR
45	NC	NC	NC	NC	E7#	E7#	CONTROL INPUT <sup>2</sup>
46	NC	NC	NC	NC	E5#	E5#	CONTROL INPUT <sup>2</sup>
47	NC	NC	E3#	E3#	E3#	E3#	CONTROL INPUT <sup>2</sup>
48	E1#	E1#	E1#	E1#	E1#	E1#	CONTROL INPUT
49	VDD1	VDD1	VDD1	VDD1	VDD1	VDD1	PWR
50	G#	G#	G#	G#	G#	G#	CONTROL INPUT
51	VSS	VSS	VSS	VSS	VSS	VSS	PWR
52	E2#	E2#	E2#	E2#	E2#	E2#	CONTROL INPUT
53	NC	NC	E4#	E4#	E4#	E4#	CONTROL INPUT <sup>2</sup>

Table 2. Device Option: Signal and Pin Description

Pkg Pin #	UT8ER1M32M (Master) Signal Name	UT8ER1M32S (Slave) Signal Name	UT8ER2M32M (Master) Signal Name	UT8ER2M32S (Slave) Signal Name	UT8ER4M32M (Master) Signal Name	UT8ER4M32S (Slave) Signal Name	Device Pin Description
54	NC	NC	NC	NC	E6#	E6#	CONTROL INPUT <sup>2</sup>
55	NC	NC	NC	NC	E8#	E8#	CONTROL INPUT <sup>2</sup>
56	VDD1	VDD1	VDD1	VDD1	VDD1	VDD1	PWR
57	SCRUB#	SCRUB#	SCRUB#	SCRUB#	SCRUB#	SCRUB#	CONTROL I/O <sup>3</sup>
58	MBE	MBE	MBE	MBE	MBE	MBE	DATA I/O
59	VDD2	VDD2	VDD2	VDD2	VDD2	VDD2	PWR
60	NC	NC	NC	NC	NC	NC	NC
61	NC	NC	NC	NC	NC	NC	NC
62	VSS	VSS	VSS	VSS	VSS	VSS	PWR
63	A14	A14	A14	A14	A14	A14	ADDRESS INPUT
64	A15	A15	A15	A15	A15	A15	ADDRESS INPUT
65	A16	A16	A16	A16	A16	A16	ADDRESS INPUT
66	VSS	VSS	VSS	VSS	VSS	VSS	PWR
67	VSS	VSS	VSS	VSS	VSS	VSS	PWR
68	VSS	VSS	VSS	VSS	VSS	VSS	PWR
69	DQ31	DQ31	DQ31	DQ31	DQ31	DQ31	DATA I/O
70	DQ30	DQ30	DQ30	DQ30	DQ30	DQ30	DATA I/O
71	DQ29	DQ29	DQ29	DQ29	DQ29	DQ29	DATA I/O
72	DQ28	DQ28	DQ28	DQ28	DQ28	DQ28	DATA I/O
73	VDD2	VDD2	VDD2	VDD2	VDD2	VDD2	PWR
74	VSS	VSS	VSS	VSS	VSS	VSS	PWR
75	DQ27	DQ27	DQ27	DQ27	DQ27	DQ27	DATA I/O
76	DQ26	DQ26	DQ26	DQ26	DQ26	DQ26	DATA I/O
77	DQ25	DQ25	DQ25	DQ25	DQ25	DQ25	DATA I/O
78	DQ24	DQ24	DQ24	DQ24	DQ24	DQ24	DATA I/O
79	VDD1	VDD1	VDD1	VDD1	VDD1	VDD1	PWR
80	VSS	VSS	VSS	VSS	VSS	VSS	PWR

Table 2. Device Option: Signal and Pin Description

Pkg Pin #	UT8ER1M32M (Master) Signal Name	UT8ER1M32S (Slave) Signal Name	UT8ER2M32M (Master) Signal Name	UT8ER2M32S (Slave) Signal Name	UT8ER4M32M (Master) Signal Name	UT8ER4M32S (Slave) Signal Name	Device Pin Description
81	NC	NC	NC	NC	NC	NC	NC
82	VDD2	VDD2	VDD2	VDD2	VDD2	VDD2	PWR
83	NC	NC	NC	NC	NC	NC	NC
84	VDD2	VDD2	VDD2	VDD2	VDD2	VDD2	PWR
85	NC	NC	NC	NC	NC	NC	NC
86	VSS	VSS	VSS	VSS	VSS	VSS	PWR
87	VDD1	VDD1	VDD1	VDD1	VDD1	VDD1	PWR
88	DQ23	DQ23	DQ23	DQ23	DQ23	DQ23	DATA I/O
89	DQ22	DQ22	DQ22	DQ22	DQ22	DQ22	DATA I/O
90	DQ21	DQ21	DQ21	DQ21	DQ21	DQ21	DATA I/O
91	DQ20	DQ20	DQ20	DQ20	DQ20	DQ20	DATA I/O
92	VSS	VSS	VSS	VSS	VSS	VSS	PWR
93	VDD2	VDD2	VDD2	VDD2	VDD2	VDD2	PWR
94	DQ19	DQ19	DQ19	DQ19	DQ19	DQ19	DATA I/O
95	DQ18	DQ18	DQ18	DQ18	DQ18	DQ18	DATA I/O
96	DQ17	DQ17	DQ17	DQ17	DQ17	DQ17	DATA I/O
97	DQ16	DQ16	DQ16	DQ16	DQ16	DQ16	DATA I/O
98	VSS	VSS	VSS	VSS	VSS	VSS	PWR
99	VSS	VSS	VSS	VSS	VSS	VSS	PWR
100	VSS	VSS	VSS	VSS	VSS	VSS	PWR
101	VSS	VSS	VSS	VSS	VSS	VSS	PWR
102	A10	A10	A10	A10	A10	A10	ADDRESS INPUT
103	A9	A9	A9	A9	A9	A9	ADDRESS INPUT
104	A8	A8	A8	A8	A8	A8	ADDRESS INPUT
105	A7	A7	A7	A7	A7	A7	ADDRESS INPUT
106	VDD1	VDD1	VDD1	VDD1	VDD1	VDD1	PWR
107	VSS	VSS	VSS	VSS	VSS	VSS	PWR
108	A6	A6	A6	A6	A6	A6	ADDRESS INPUT

Table 2. Device Option: Signal and Pin Description

Pkg Pin #	UT8ER1M32M (Master) Signal Name	UT8ER1M32S (Slave) Signal Name	UT8ER2M32M (Master) Signal Name	UT8ER2M32S (Slave) Signal Name	UT8ER4M32M (Master) Signal Name	UT8ER4M32S (Slave) Signal Name	Device Pin Description
109	W#	W#	W#	W#	W#	W#	CONTROL INPUT
110	A18	A18	A18	A18	A18	A18	ADDRESS INPUT
111	NC	NC	NC	NC	NC	NC	NC
112	VDD1	VDD1	VDD1	VDD1	VDD1	VDD1	PWR
113	NC	NC	NC	NC	NC	NC	NC
114	NC	NC	NC	NC	NC	NC	NC
115	VDD1	VDD1	VDD1	VDD1	VDD1	VDD1	PWR
116	NC	NC	NC	NC	NC	NC	NC
117	VSS	VSS	VSS	VSS	VSS	VSS	PWR
118	NC	NC	NC	NC	NC	NC	NC
119	NC	NC	NC	NC	NC	NC	NC
120	VDD1	VDD1	VDD1	VDD1	VDD1	VDD1	PWR
121	NC	NC	NC	NC	NC	NC	NC
122	A17	A17	A17	A17	A17	A17	ADDRESS INPUT
123	A5	A5	A5	A5	A5	A5	ADDRESS INPUT
124	A4	A4	A4	A4	A4	A4	ADDRESS INPUT
125	VSS	VSS	VSS	VSS	VSS	VSS	PWR
126	VDD1	VDD1	VDD1	VDD1	VDD1	VDD1	PWR
127	A3	A3	A3	A3	A3	A3	ADDRESS INPUT
128	A2	A2	A2	A2	A2	A2	ADDRESS INPUT
129	A1	A1	A1	A1	A1	A1	ADDRESS INPUT
130	A0	A0	A0	A0	A0	A0	ADDRESS INPUT
131	VSS	VSS	VSS	VSS	VSS	VSS	PWR
132	VSS	VSS	VSS	VSS	VSS	VSS	PWR

**Notes:**

NC Pins are not connected on the die

1. BUSY# pin is an output for master devices only, and is a NC for slave devices.

2. Control input when shown as En#, otherwise pin is NC.

3. SCRUB# is an output for master devices, but an input for slave devices.



## MASTER or SLAVE OPTIONS

To reduce the bit error rates, the SRAM devices employ an embedded EDAC (error detection and correction) with user programmable auto scrubbing options. The SRAM devices can automatically correct single bit word errors in event of an upset. During a read operation, if a multiple bit error occurs in a word, the SRAMs assert the MBE output to notify the host.

All SRAM devices are offered in two options: Master (UT8ER1M32M, UT8ER2M32M and UT8ER4M32M) or Slave (UT8ER1M32S, UT8ER2M32S and UT8ER4M32S). The masters are a full function device which features user defined autonomous EDAC scrubbing options. The slave device employs a scrub on demand feature.

The master and slave device pins  $\overline{\text{SCRUB}}$  and  $\overline{\text{BUSY}}$  are physically different. The  $\overline{\text{SCRUB}}$  pin is an output on the master device, but an input on the slave device. The master  $\overline{\text{SCRUB}}$  pin asserts low when a scrub cycle initiates, and can be used to demand scrub cycles from multiple slave units when connected to the  $\overline{\text{SCRUB}}$  input of slave(s). The  $\overline{\text{BUSY}}$  pin is an output for the master device and can be used to generate wait states by the memory controller. The  $\overline{\text{BUSY}}$  pin is a no connect (NC) for slave devices.

## DEVICE OPERATION

The SRAMs have control inputs called Chip Enable ( $\overline{\text{En}}$ ), Write Enable ( $\overline{\text{W}}$ ), and Output Enable ( $\overline{\text{G}}$ ); 19 address inputs, A(18:0); and 32 bidirectional data lines, DQ(31:0). The  $\overline{\text{En}}$  (chip enable) controls selection between active and standby modes. Asserting  $\overline{\text{En}}$  enables the device, causes  $I_{\text{DD}}$  to rise to its active value, and decodes the 19 address inputs. Only one chip enable may be active at any time.  $\overline{\text{W}}$  controls read and write operations. During a read cycle,  $\overline{\text{G}}$  must be asserted to enable the outputs.

**Table 3. SRAM Device Control Operation Truth Table**

$\overline{\text{G}}$	$\overline{\text{W}}$	$\overline{\text{En}}$	I/O Mode	Mode
X	X	H	DQ(31:0) 3-State	Standby
L	H	L	DQ(31:0) Data Out	Word Read
H	H	L	DQ(31:0) All 3-State	Word Read <sup>2</sup>
X	L	L	DQ(31:0) All 3-State	Word Write

**Notes:**

1. "X" is defined as a "don't care" condition.
2. Device active; outputs disabled.

**Table 4. EDAC Control Pin Operation Truth Table**

MBE	$\overline{\text{SCRUB}}$	$\overline{\text{BUSY}}$	I/O Mode	Mode
H	H	H	Read	Uncorrectable Multiple Bit Error
L	H	H	Read	Valid Data Out
X	H	H	X	Device Ready
X	H	L	X	Device Ready / Scrub Request Pending
X	L	X	Not Accessible	Device Busy

**Notes:**

1. "X" is defined as a "don't care" condition
2.  $\overline{\text{BUSY}}$  signal is a "NC" for slave devices and are an "X" don't care.

## READ CYCLE

A combination of  $\overline{\text{W}}$  greater than  $V_{\text{IH}}$  (min) with a single  $\overline{\text{En}}$  and  $\overline{\text{G}}$  less than  $V_{\text{IL}}$  (max) defines a read cycle. Read access time is measured from the latter of device enable, output enable, or valid address to valid data output.

SRAM Read Cycle 1, the Address Access in Figure 3a, is initiated by a change in address inputs after a single  $\overline{\text{En}}$  is asserted,  $\overline{\text{G}}$  is asserted,  $\overline{\text{W}}$  is deasserted and all are stable. Valid data appears on data outputs DQ(31:0) after the specified  $t_{\text{AVQV}}$  is satisfied. Outputs remain active throughout the entire cycle. As long as device enable and output enable are active, the minimum time between valid address changes is specified by the read cycle time ( $t_{\text{AVAV}}$ ).

SRAM Read Cycle 2, the Chip Enable-controlled Access in Figure 3b is initiated by a single  $\overline{\text{En}}$  going active while  $\overline{\text{G}}$  remains asserted,  $\overline{\text{W}}$  remains deasserted, and the addresses remain stable for the entire cycle. After the specified  $t_{\text{ETQV}}$  is satisfied, the 32-bit word addressed by A(18:0) is accessed and appears at the data outputs DQ(31:0).

SRAM Read Cycle 3, the Output Enable-controlled Access in Figure 3c, is initiated by  $\overline{\text{G}}$  going active while a single  $\overline{\text{En}}$  is asserted,  $\overline{\text{W}}$  is deasserted, and the addresses are stable. Read access time is  $t_{\text{GLQV}}$  unless  $t_{\text{AVQV}}$  or  $t_{\text{ETQV}}$  (reference Figure 3b) have not been satisfied.

SRAM EDAC Status Indications during a Read Cycle, if MBE is Low, the data is valid. If MBE is High, the data is corrupted (reference Table 3).

## WRITE CYCLE

A combination of  $\overline{W}$  and a single  $\overline{En}$  less than  $V_{IL}(\max)$  defines a write cycle. The state of  $\overline{G}$  is a “don’t care” for a write cycle. The outputs are placed in the high-impedance state when either  $\overline{G}$  is greater than  $V_{IH}(\min)$  or when  $\overline{W}$  is less than  $V_{IL}(\max)$ .

Write Cycle 1, the Write Enable-controlled Access in Figure 4a, is defined by a write terminated by  $\overline{W}$  going high with a single  $\overline{En}$  still active. The write pulse width is defined by  $t_{WLWH}$  when the write is initiated by  $\overline{W}$  and by  $t_{ETWH}$  when the write is initiated by  $\overline{En}$ . To avoid bus contention  $t_{WLQZ}$  must be satisfied before data is applied to the 32 bidirectional pins DQ(31:0) unless the outputs have been previously placed in high impedance state by deasserting  $\overline{G}$ .

Write Cycle 2, the Chip Enable-controlled Access in Figure 4b, is defined by a write terminated by a single  $\overline{En}$ . The write pulse width is defined by  $t_{WLEF}$  when the write is initiated by  $\overline{W}$  and by  $t_{ETEF}$  when the write is initiated by  $\overline{En}$  going active. For the  $\overline{W}$  initiated write, unless the outputs have been previously placed in the high-impedance state by  $\overline{G}$ , the user must wait  $t_{WLQZ}$  before applying data to the 32 bidirectional pins DQ(31:0) to avoid bus contention.

## CONTROL REGISTER WRITE/READ CYCLES

Configuration options can be selected by writing to the control register. The configuration tables (Tables 5 and 6) details the programming options. Scrub rate period and  $\overline{BUSY}$  to  $\overline{SCRUB}$  configurations are applicable to master devices using  $\overline{E1}$  chip enable only. EDAC bypass and Read/Write control register is applicable to all valid chip enables  $\overline{En}$ . The control register is accessed by applying a series of values to the address bus as shown in Figures 7a and 7b. After the series the contents of the control register can be either read or written depending on the value of the corresponding read/write control register address pin (A(9) for odd die and A(2) for even die). **NOTE:** MBE must be driven high by the user for both a write or a read of the control register.

## MEMORY SCRUBBING/CYCLE STEALING

The SRAMs use architectural improvements and embedded error detection and correction to maintain unsurpassed levels of error protection. This is accomplished by what Aeroflex refers to as Cycle Stealing. To minimize the system design impact on the speed of operation, the edge relationship between  $\overline{BUSY}$  and  $\overline{SCRUB}$  is programmable via the sequence described in figures 7a and 7b. The  $\overline{BUSY}$  output is intended to give notification to the memory controller that a scrub cycle is impending. Since the memory cannot be accessed during an internal scrub cycle, the  $\overline{BUSY}$  to  $\overline{SCRUB}$  delay can be adjusted so the user may complete accesses prior to internal scrubbing.

The effective error rate is a function of the intrinsic error rate and the environment. Therefore, users are given the ability to control the scrub rate (ref. figure 7a) appropriate for the applicable environment. **NOTE:** the scrub rate will have an inverse relationship to the total throughput of the memory.

A master mode scrub cycle will occur at the user defined Scrub Rate Period. A scrub cycle is defined as the verification and correction (if necessary) of data for a single word address location. Address locations are scrubbed sequentially every Scrub Rate Period ( $t_{SCRT}$ ). Scrub cycles will occur at every Scrub Rate Period regardless of the status of control pins. All inputs should remain stable while the  $\overline{SCRUB}$  signal is active to avoid data corruption. Control pin function will be returned upon deassertion of  $\overline{BUSY}$  pin. The Slave mode scrub cycle occurs anytime the  $\overline{SCRUB}$  pin is asserted. The scrub cycle is defined the same as the master mode and will occur regardless of control pin status. Control pin function will be returned upon  $\overline{SCRUB}$  deassertion.

Data is corrected during not only the internal scrub, but again during a user requested read cycle. If the data presented contains two or more errors after  $t_{AVAV}$  is satisfied, the MBE signal will be asserted. (**Note:** Reading un-initialized memory locations may result in un-intended MBE assertions.)

**Table 5. Operational Environment<sup>1</sup>**

Total Dose	100k	rads(Si)
Heavy Ion Error Rate <sup>2</sup>	$8.1 \times 10^{-16}$	Errors/Bit-Day

### Notes:

1. The SRAM is immune to latchup to particles  $\leq 110\text{MeV}\cdot\text{cm}^2/\text{mg}$ .
2. 90% worst case particle environment, Geosynchronous orbit, 100 mils of Aluminum and default EDAC scrub rate.

## SUPPLY SEQUENCING

No supply voltage sequencing is required between  $V_{DD1}$  and  $V_{DD2}$ .

## POWER-UP REQUIREMENTS

During power-up of the SRAM devices, the power supply voltages will transverse through voltage ranges where the device is not guaranteed to operate before reaching final levels. Since some circuits on the device may operate at lower voltage levels than others, the device may power-up in an unknown state. To eliminate this with most power-up situations, the device employs an on-chip power-on-reset (POR) circuit. The POR, however, requires time to complete the operation. Therefore, it is recommended that all device activity be delayed by a minimum of 100ms, after both  $V_{DD1}$  and  $V_{DD2}$  supplies have reached stable minimum operating voltage.

**ABSOLUTE MAXIMUM RATINGS<sup>1</sup>**(Referenced to  $V_{SS}$ )

SYMBOL	PARAMETER	LIMITS
$V_{DD1}$	DC supply voltage (Core)	-0.3 to 2.1V
$V_{DD2}$	DC supply voltage (I/O)	-0.3 to 3.8V
$V_{I/O}$	Voltage on any pin	-0.3 to 3.8V
$T_{STG}$	Storage temperature	-65 to +150°C
$P_D$ <sup>2</sup> : UT8ER1M32 UT8ER2M32 UT8ER4M32	Maximum package power dissipation permitted @ $T_c = +105^\circ\text{C}$	3.3W 2W 1.3W
$T_J$	Maximum junction temperature	+150°C
$\Theta_{JC}$ <sup>3</sup> : UT8ER1M32 UT8ER2M32 UT8ER4M32	Thermal resistance, junction-to-case <sup>2</sup>	6°C/W 10°C/W 15°C/W
$I_I$	DC input current	±10 mA

**Notes:**

- Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
- Per MIL-STD-883, Method 1012, Section 3.4.1,  $P_D = \frac{(125^\circ\text{C} - 105^\circ\text{C})}{\Theta_{JC}}$
- $\Theta_{JC}$  varies with density due to stacked die configuration.

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	LIMITS
$V_{DD1}$	DC supply voltage (Core)	1.7 to 2.0V
$V_{DD2}$	DC supply voltage (I/O)	2.3 to 3.6V
$T_C$	Case temperature range	-55 to +105°C
$V_{IN}$	DC input voltage	0V to $V_{DD2}$

**DC ELECTRICAL CHARACTERISTICS (Pre and Post-Radiation)\***(V<sub>DD1</sub> = 1.7V to 2.0V, V<sub>DD2</sub> = 2.3V to 3.6V; Unless otherwise noted, T<sub>c</sub> is per the temperature range ordered)

SYMBOL	PARAMETER	CONDITION		MIN	MAX	UNIT
V <sub>IH</sub>	High-level input voltage			2.2		V
V <sub>IL</sub>	Low-level input voltage				0.8	V
V <sub>OL1</sub> <sup>1</sup>	Low-level output voltage	I <sub>OL</sub> = 8mA, 3.0V ≤ V <sub>DD2</sub> ≤ 3.6V			0.4	V
V <sub>OL2</sub> <sup>1</sup>	Low-level output voltage	I <sub>OL</sub> = 6mA, 2.3V ≤ V <sub>DD2</sub> ≤ 2.7V			0.2*V <sub>DD2</sub>	
V <sub>OH1</sub>	High-level output voltage	I <sub>OH</sub> = -4mA, 3.0V ≤ V <sub>DD2</sub> ≤ 3.6V		0.8*V <sub>DD2</sub>		V
V <sub>OH2</sub>	High-level output voltage	I <sub>OL</sub> = -2mA, 2.3V ≤ V <sub>DD2</sub> ≤ 2.7V		0.8*V <sub>DD2</sub>		V
I <sub>IN</sub>	Input leakage current	V <sub>IN</sub> = V <sub>DD2</sub> and V <sub>SS</sub>		-2	2	μA
I <sub>OZ</sub> <sup>3</sup>	Three-state output leakage current	V <sub>O</sub> = V <sub>DD2</sub> and V <sub>SS</sub> V <sub>DD2</sub> = V <sub>DD2</sub> (max), $\bar{G}$ = V <sub>DD2</sub> (max)		-2	2	μA
I <sub>OS</sub> <sup>4, 5</sup>	Short-circuit output current	V <sub>DD2</sub> = V <sub>DD2</sub> (max), V <sub>O</sub> = V <sub>DD2</sub> V <sub>DD2</sub> = V <sub>DD2</sub> (max), V <sub>O</sub> = V <sub>SS</sub>		-100	+100	mA
I <sub>DD1</sub> (OP <sub>1</sub> <sup>6,8</sup> )	V <sub>DD1</sub> Supply current read operation @ 1MHz, EDAC enabled @ default Scrub Rate Period (see table 5).	Inputs: V <sub>IL</sub> = V <sub>SS</sub> + 0.2V, V <sub>IH</sub> = V <sub>DD2</sub> - 0.2V, I <sub>OUT</sub> = 0 V <sub>DD1</sub> = V <sub>DD1</sub> (max), V <sub>DD2</sub> = V <sub>DD2</sub> (max)	V <sub>DD1</sub> = 2.0V		14	mA
			V <sub>DD1</sub> = 1.9V		10	mA
I <sub>DD1</sub> (OP <sub>2</sub> <sup>6,8,9</sup> )	V <sub>DD1</sub> Supply current read operation @ f <sub>max</sub> , EDAC enabled @ default Scrub Rate Period (see table 5).	Inputs: V <sub>IL</sub> = V <sub>SS</sub> + 0.2V, V <sub>IH</sub> = V <sub>DD2</sub> - 0.2V, I <sub>OUT</sub> = 0 V <sub>DD1</sub> = V <sub>DD1</sub> (max), V <sub>DD2</sub> = V <sub>DD2</sub> (max)	V <sub>DD1</sub> = 2.0V V <sub>DD1</sub> = 1.9V UT8ER4M32		230 215	mA mA
			V <sub>DD1</sub> = 2.0V V <sub>DD1</sub> = 1.9V UT8ER1M32 UT8ER2M32		225 210	mA mA
I <sub>DD2</sub> (OP <sub>1</sub> <sup>6,8</sup> )	V <sub>DD2</sub> Supply current read operation @ 1MHz, EDAC enabled @ default Scrub Rate Period (see table 5).	Inputs : V <sub>IL</sub> = V <sub>SS</sub> + 0.2V, V <sub>IH</sub> = V <sub>DD2</sub> - 0.2V, I <sub>OUT</sub> = 0 V <sub>DD1</sub> = V <sub>DD1</sub> (max), V <sub>DD2</sub> = V <sub>DD2</sub> (max)			2	mA
I <sub>DD2</sub> (OP <sub>2</sub> <sup>6,8,9</sup> )	V <sub>DD2</sub> Supply current read operation @ f <sub>max</sub> , EDAC enabled @ default Scrub Rate Period (see table 5).	Inputs : V <sub>IL</sub> = V <sub>SS</sub> + 0.2V, V <sub>IH</sub> = V <sub>DD2</sub> - 0.2V, I <sub>OUT</sub> = 0 V <sub>DD1</sub> = V <sub>DD1</sub> (max), V <sub>DD2</sub> = V <sub>DD2</sub> (max)			5	mA

SYMBOL	PARAMETER	CONDITION		MIN	MAX	UNIT
$I_{DD1}(SB)^{7,10}$	Supply current standby @ 0Hz, EDAC disabled (per die)	CMOS inputs, $I_{OUT} = 0$ $\overline{E_n} = V_{DD2} - 0.2$ $V_{DD1} = V_{DD1}(\text{max}), V_{DD2} = V_{DD2}(\text{max})$	-55°C and 25°C		15	mA
			105°C		35	mA
$I_{DD2}(SB)^{10}$	Supply current standby @ 0Hz, EDAC disabled (per die)	CMOS inputs, $I_{OUT} = 0$ $\overline{E_n} = V_{DD2} - 0.2$ $V_{DD1} = V_{DD1}(\text{max}), V_{DD2} = V_{DD2}(\text{max})$			3	mA
$I_{DD1}(SB)^{7,9,10}$	Supply current standby A(16:0) @ fmax, EDAC disabled (per die)	CMOS inputs, $I_{OUT} = 0$ $\overline{E_n} = V_{DD2} - 0.2$ $V_{DD1} = V_{DD1}(\text{max}), V_{DD2} = V_{DD2}(\text{max})$	-55°C and 25°C		15	mA
			105°C		35	mA
$I_{DD2}(SB)^{9,10}$	Supply current standby A(16:0) @ fmax, EDAC disabled (per die)	CMOS inputs, $I_{OUT} = 0$ $\overline{E_n} = V_{DD2} - 0.2$ $V_{DD1} = V_{DD1}(\text{max}), V_{DD2} = V_{DD2}(\text{max})$			3	mA

## CAPACITANCE

SYMBOL	PARAMETER	CONDITION	UT8ER1M32		UT8ER2M32		UT8ER4M32		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$C_{IN}^2$	Input capacitance	$f = 1\text{MHz} @ 0V$		18		29		50	pF
$C_{En}^2$	Input capacitance Device Enables	$f = 1\text{MHz} @ 0V$		10		10		10	pF
$C_{IO}^2$	Bidirectional I/O capacitance	$f = 1\text{MHz} @ 0V$		15		27		50	pF

### Notes:

\* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

- The SCRUB and BUSY pins for UT8ER1M32M, UT8ER2M32M and UT8ER4M32M (master) are tested functionally for VOL specification.
- Measured only for initial qualification and after process or design changes that could affect this parameter.
- The SCRUB and BUSY pins for UT8ER1M32M, UT8ER2M32M and UT8ER4M32M (master) are guaranteed by design, but neither tested nor characterized.
- Supplied as a design limit but not guaranteed or tested.
- Not more than one output may be shorted at a time for maximum duration of one second.
- EDAC enabled. Default Scrub Rate Period applicable to master device only.
- Post radiation limits are the 105°C temperature limit when specified.
- Operating current limit does not include standby current.
- fmax = 50MHz.
- $V_{IH} = V_{DD2}(\text{max}), V_{IL} = 0V$ .

**AC CHARACTERISTICS READ CYCLE (Pre and Post-Radiation)\***(V<sub>DD1</sub> = 1.7V to 2.0V, V<sub>DD2</sub> = 2.3V to 3.6V); Unless otherwise noted, Tc is per the temperature range ordered

SYMBOL	PARAMETER	UT8ER1M32		UT8ER2M32		UT8ER4M32		UNIT	FIGURE
		MIN	MAX	MIN	MAX	MIN	MAX		
t <sub>AVAV1</sub> <sup>1</sup>	Read cycle time	20		22		25		ns	3a
t <sub>AVQV1</sub>	Address to data valid from address change		20		22		25	ns	3c
t <sub>AXQX</sub> <sup>2</sup>	Output hold time	1.5		1.5		1.5		ns	3a
t <sub>GLQX</sub> <sup>1,2</sup>	$\overline{G}$ -controlled output enable time	1		1		1		ns	3c
t <sub>GLQV</sub>	$\overline{G}$ -controlled output data valid		10		10		10	ns	3c
t <sub>GHQZ1</sub> <sup>2</sup>	$\overline{G}$ -controlled output three-state time	1	8	1	8	1	8	ns	3c
t <sub>ETQX</sub> <sup>2</sup>	E-controlled output enable time	4		4		4		ns	3b
t <sub>ETQV</sub>	E-controlled access time		20		22		25	ns	3b
t <sub>EFQZ</sub> <sup>2</sup>	E-controlled output three-state time <sup>2</sup>	2	9	2	9	2	9	ns	3b
t <sub>AVMV</sub>	Address to error flag valid		22		22		25	ns	3a
t <sub>AXMX</sub> <sup>2</sup>	Address to error flag hold time from address change	1.5		1.5		1.5		ns	3a
t <sub>GLMX</sub> <sup>2</sup>	$\overline{G}$ -controlled error flag enable time	0		0		0		ns	3c
t <sub>GLMV</sub>	$\overline{G}$ -controlled error flag valid		8		8		8	ns	3c
t <sub>ETMX</sub> <sup>2</sup>	E-controlled error flag enable time	4		4		4		ns	3b
t <sub>ETMV</sub>	E-controlled error flag time		22		22		25	ns	3b
t <sub>GHMZ</sub> <sup>2</sup>	G-controlled error flag three-state time	1	9	1	9	1	9	ns	3b

**Notes:**

\* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1. Guaranteed by characterization, but not tested.

2. Three-state is defined as a change from steady-state output voltage.

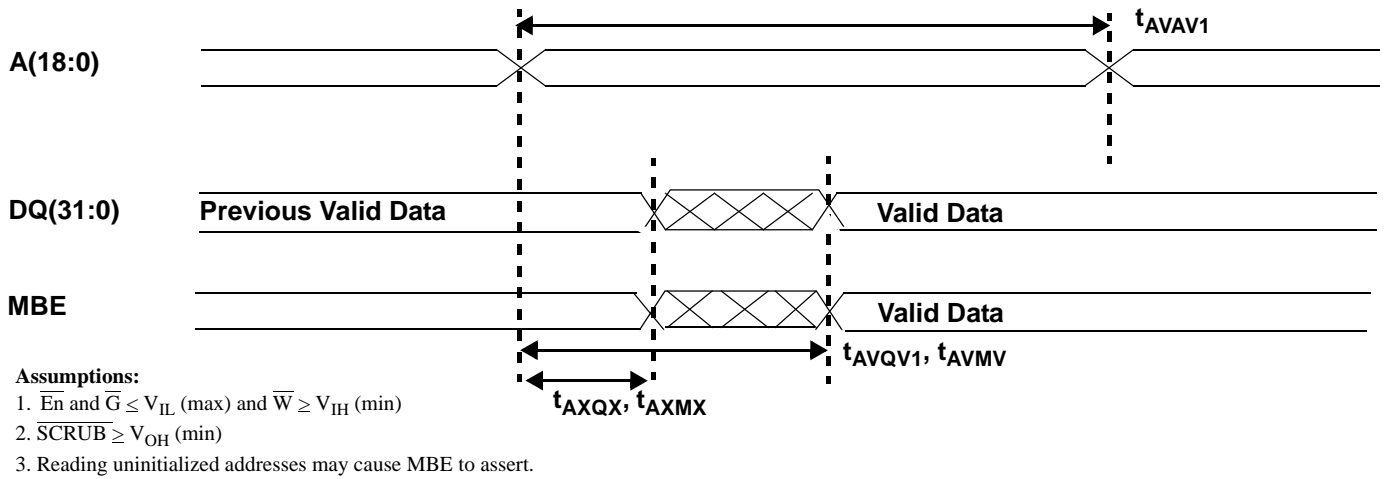


Figure 3a. SRAM Read Cycle 1: Address Access

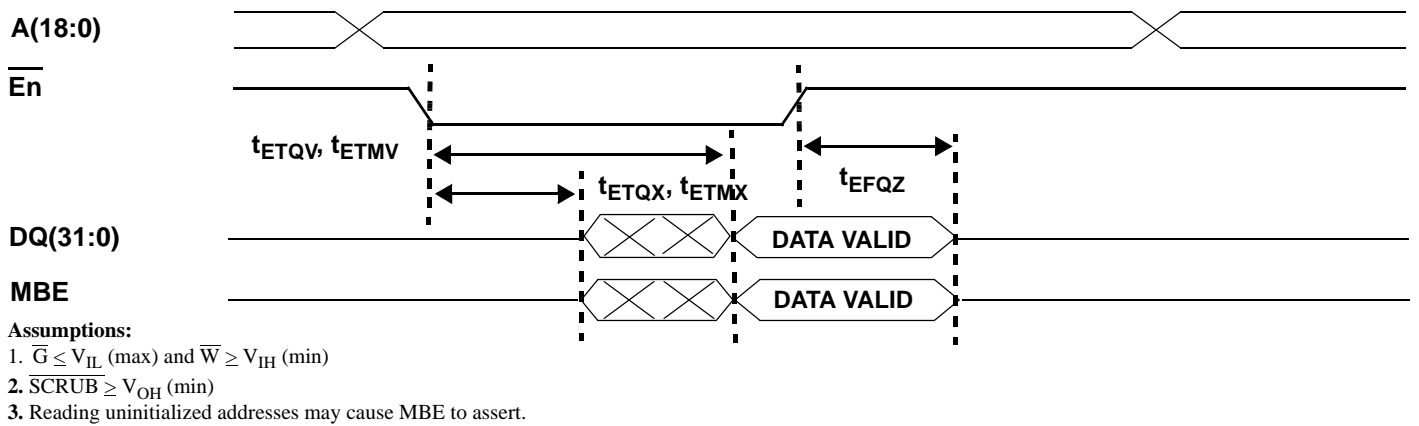


Figure 3b. SRAM Read Cycle 2: Chip Enable Access

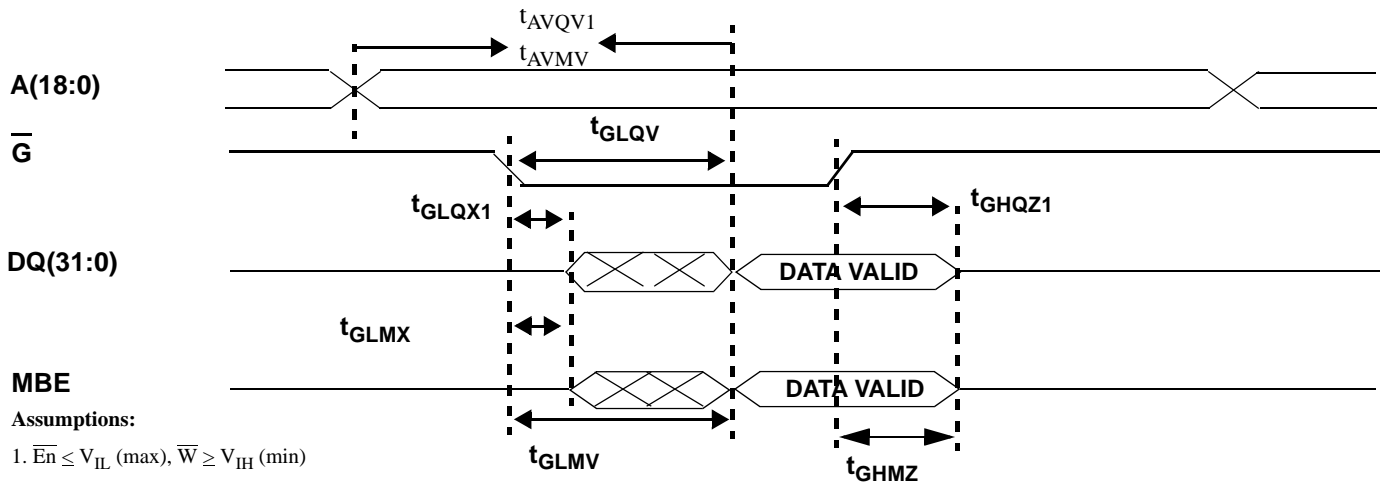


Figure 3c. SRAM Read Cycle 3: Output Enable Access

**AC CHARACTERISTICS WRITE CYCLE (Pre and Post-Radiation)\***(V<sub>DD1</sub> = 1.7V to 2.0V, V<sub>DD2</sub> = 2.3V to 3.6V); Unless otherwise noted, T<sub>c</sub> is per the temperature range ordered

SYMBOL	PARAMETER	UT8ER1M32		UT8ER2M32		UT8ER4M32		UNIT	FIGURE
		MIN	MAX	MIN	MAX	MIN	MAX		
t <sub>AVAV2</sub> <sup>1</sup>	Write cycle time	10		10		10		ns	4a/4b
t <sub>ETWH</sub>	Device enable to end of write	10		10		10		ns	4a
t <sub>AVET</sub>	Address setup time for write ( $\overline{E}n$ - controlled)	0		0		0		ns	4b
t <sub>AVWL</sub>	Address setup time for write ( $\overline{W}$ - controlled)	0		0		0		ns	4a
t <sub>WLWH</sub> <sup>1</sup>	Write pulse width	8		8		8		ns	4a
t <sub>WHAX</sub>	Address hold time for write ( $\overline{W}$ - controlled)	0		0		0		ns	4a
t <sub>EFAX</sub>	Address hold time for device enable ( $\overline{E}n$ - controlled)	0		0		0		ns	4b
t <sub>WLQZ</sub> <sup>2</sup>	$\overline{W}$ - controlled three-state time		9		9		9	ns	4a/4b
t <sub>WHQX</sub> <sup>2</sup>	$\overline{W}$ - controlled output enable time	0		0		0		ns	4a
t <sub>ETEF</sub>	Device enable pulse width ( $\overline{E}n$ - controlled)	10		10		10		ns	4b
t <sub>DVWH</sub>	Data setup time	5		5		6		ns	4a
t <sub>WHDX</sub>	Data hold time	0		0		0		ns	4a
t <sub>WLEF</sub> <sup>1</sup>	Device enable controlled write pulse width	8		8		8		ns	4b
t <sub>DVEF</sub>	Data setup time	5		5		6		ns	4a/4b
t <sub>EFDX</sub>	Data hold time	0		0		0		ns	4b
t <sub>AVWH</sub>	Address valid to end of write	10		10		10		ns	4a
t <sub>WHWL</sub> <sup>1</sup>	Write disable time	2		2		3		ns	4a

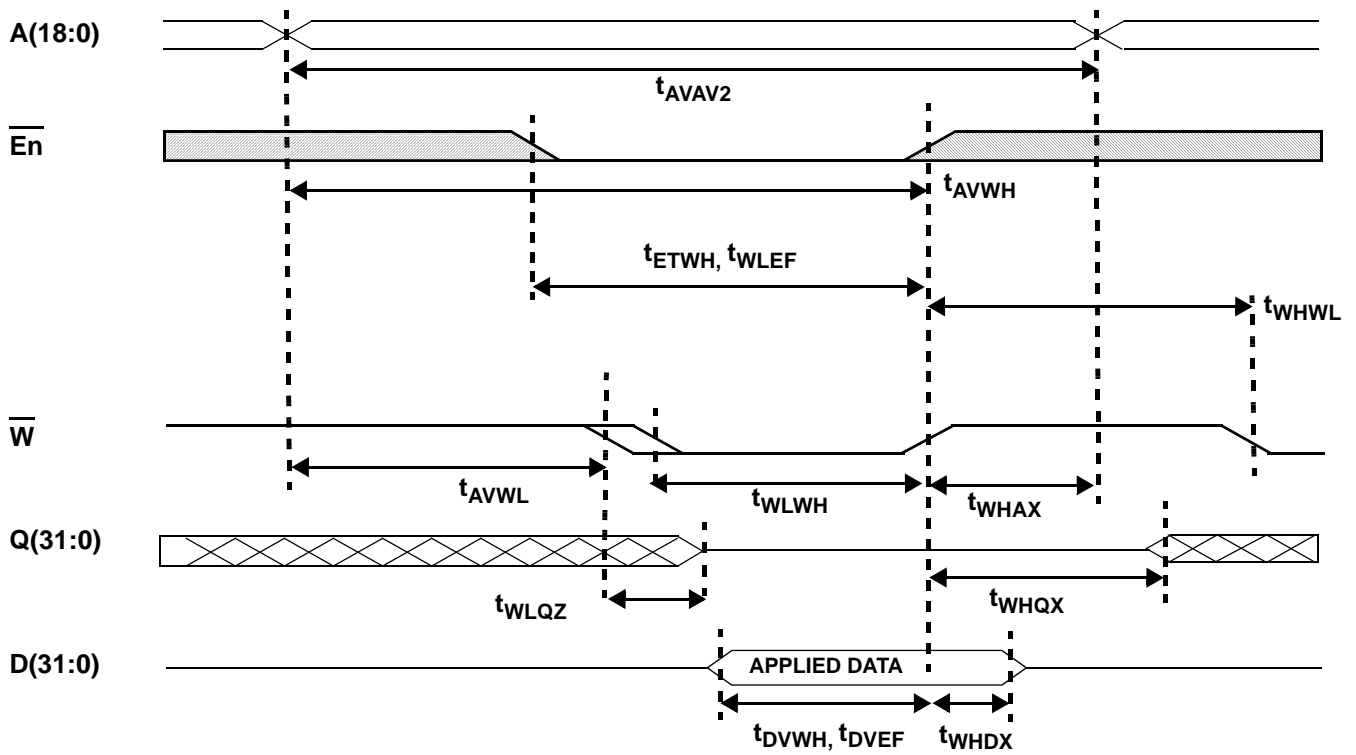
**Notes:**

\* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1. Tested with  $\overline{G}$  high.

2. Three-state is defined as a change from steady-state output voltage.

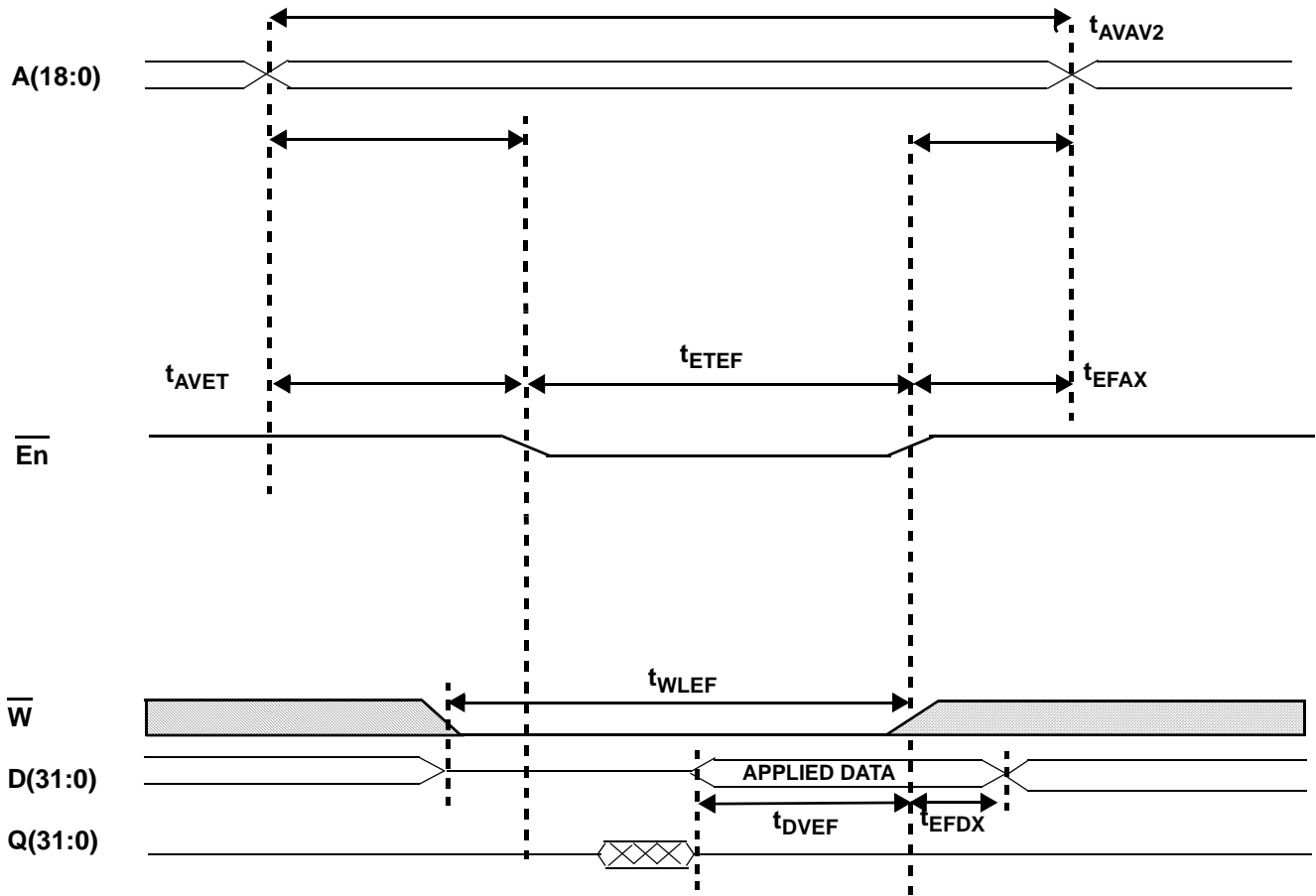




**Assumptions:**

1.  $\overline{G} \leq V_{IL}(\text{max})$ . (If  $\overline{G} \geq V_{IH}(\text{min})$  then  $Q(31:0)$  and MBE will be in three-state for the entire cycle.)
2.  $\overline{SCRUB} \geq V_{OH}(\text{min})$

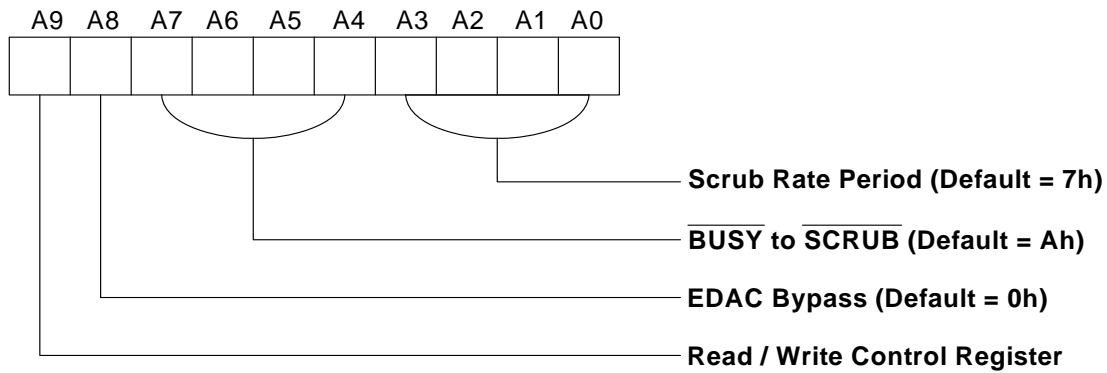
**Figure 4a. SRAM Write Cycle 1:  $\overline{W}$  - Controlled Access**



**Assumptions & Notes:**

1.  $\overline{G} \leq V_{IL}(\text{max})$ . (If  $\overline{G} \geq V_{IH}(\text{min})$  then Q(31:0) and MBE will be in three-state for the entire cycle.)
2.  $\overline{\text{Busy}} \geq V_{OH}(\text{min})$

**Figure 4b. SRAM Write Cycle 2: Enable - Controlled Access**



Note:  
1. See Table 5 for Control Register Definitions

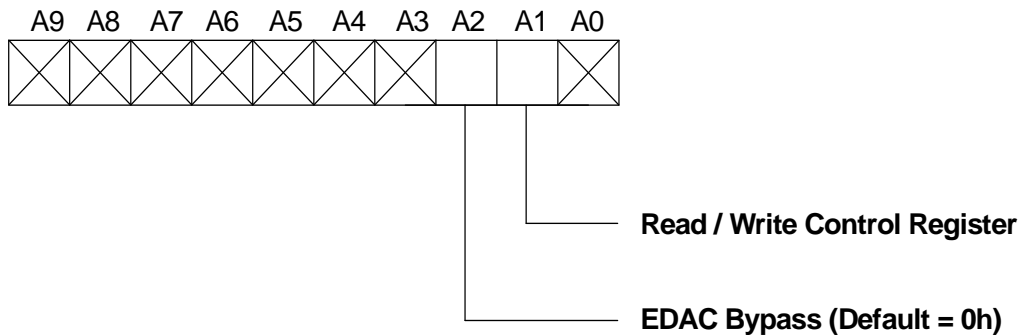
Figure 5. (Odd Die Numbers ( $\overline{E1}$ ,  $\overline{E3}$ ,  $\overline{E5}$ ,  $\overline{E7}$  Chip Enables) EDAC Control Register

Table 6: (Odd Die Numbers ( $\overline{E1}$ ,  $\overline{E3}$ ,  $\overline{E5}$ ,  $\overline{E7}$  Chip Enables) EDAC Programming Configuration Table

ADDR BIT	PARAMETER	VALUE	FUNCTION
A (3-0)	Scrub Rate Period <sup>1,2,3</sup>	3-15  Note: 0-2 reserved	As Scrub Rate Period changes from 0 - 15, then the interval between Scrub cycles will change as follows: 3 = 600 ns      8 = 13.0 us      12 = 205 us 4 = 1000 ns      9 = 25.8 us      13 = 409.8 us <sup>4</sup> 5 = 1800 ns      10 = 51.4 us      14 = 819.4 us <sup>4</sup> 6 = 3400 ns      11 = 102.6 us      15 = 1.64 ms <sup>4</sup> 7 = 6600 ns
A (7-4)	$\overline{BUSY}$ to $\overline{SCRUB}$ <sup>1,3,5</sup>	0-15	If $\overline{BUSY}$ to $\overline{SCRUB}$ changes from 0 - 15, then the interval $t_{BLSL}$ between $\overline{SCRUB}$ and $\overline{BUSY}$ will change as follows: 0 = 0 ns      6 = 300 ns      11 = 550 ns 1 = 50 ns      7 = 350 ns      12 = 600 ns 2 = 100 ns      8 = 400 ns      13 = 650 ns 3 = 150 ns      9 = 450 ns      14 = 700 ns 4 = 200 ns      10 = 500 ns      15 = 750 ns 5 = 250ns
A (8)	Bypass EDAC Bit <sup>6,7</sup>	0, 1	If 0, then normal EDAC operation will occur. If 1, then EDAC will be bypassed and no memory scrubbing will occur.
A (9)	Read / $\overline{Write}$ Control Register	0, 1	0 = A8 to A0 will be written to the control register. 1 = Control register will be asserted to the data bus DQ[8:0] respectively.

**Notes:**

1. Values based on minimum specifications. For guaranteed ranges of Scrub Rate Period ( $t_{SCRUB}$ ) and  $\overline{BUSY}$  to  $\overline{SCRUB}$  ( $t_{BLSL}$ ), reference the Master Mode AC Characteristic.
2. Default Scrub Rate Period is 6600 ns.
3. Scrub Rate Period and  $\overline{BUSY}$  to  $\overline{SCRUB}$  applicable to the master devices die #1 ( $\overline{E1}$  chip enable) only.
4. Period below test capability.
5. The default for  $t_{BLSL}$  is 500 ns.
6. The default state for A8 is 0.
7. The EDAC bypass option is provided for memory accesses when error correction is not desired (i.e. device and system testing).



Note:

X = Not applicable for even die.

1. See Table 6 for Control Register Definitions

**Figure 6. Even Die Numbers ( $\overline{E2}$ ,  $\overline{E4}$ ,  $\overline{E6}$ ,  $\overline{E8}$  Chip Enables) EDAC Control Register**

**Table 7: Even Die Numbers ( $\overline{E2}$ ,  $\overline{E4}$ ,  $\overline{E6}$ ,  $\overline{E8}$  Chip Enables) EDAC Programming Configuration Table**

ADDR BIT	PARAMETER	VALUE	FUNCTION
A (2)	Bypass EDAC Bit <sup>1,2</sup>	0, 1	If 0, then normal EDAC operation will occur. If 1, then EDAC will be bypassed and no memory scrubbing will occur.
A (1)	Read / $\overline{\text{Write}}$ Control Register	0, 1	0 = A2 will be written to the control register 1 = Control register will be asserted to the data bus DQ18

Notes:

1. The default state for A2 is 0.

2. The EDAC bypass option is provided for memory accesses when error correction is not desired (i.e. device and system testing).

**EDAC CONTROL REGISTER AC CHARACTERISTICS (Pre and Post-Radiation)\***

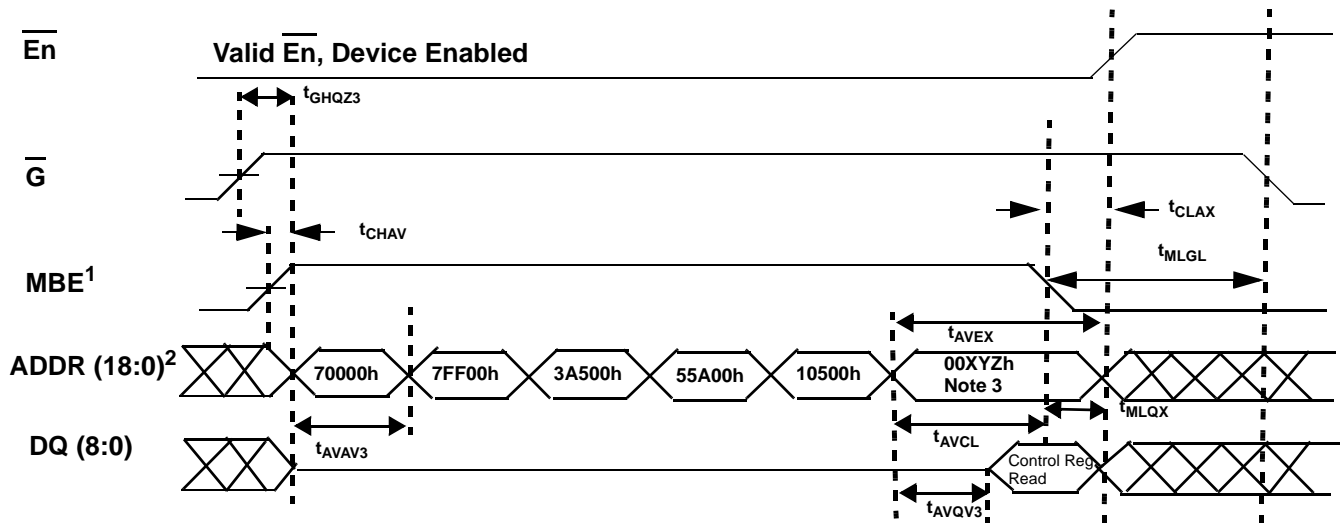
(V<sub>DD1</sub> = 1.7V to 2.0V, V<sub>DD2</sub> = 2.3V to 3.6V); Unless otherwise noted, T<sub>c</sub> is per the temperature range ordered

SYMBOL	PARAMETER	UT8ER1M32 UT8ER2M32 UT8ER4M32		UNIT	FIGURE
		MIN	MAX		
t <sub>AVAV3</sub>	Address valid to address valid for control register cycle	200		ns	7a, 7b
t <sub>AVCL</sub>	Address valid to control low	400		ns	7a, 7b
t <sub>AVEX</sub>	Address valid to enable de-assertion	200		ns	7a, 7b
t <sub>AVQV3</sub>	Address to data valid control register read		400	ns	7a, 7b
t <sub>MLQX</sub> <sup>1</sup>	MBE control EDAC disable time	3		ns	7a, 7b
t <sub>CHAV</sub>	MBE high to address valid	0		ns	7a, 7b
t <sub>CLAX</sub>	MBE low to address invalid	0		ns	7a, 7b
t <sub>GHQZ3</sub> <sup>1</sup>	Output tri-state time	2	9	ns	7a, 7b
t <sub>MLGL</sub> <sup>2</sup>	MBE low to output enable	85		ns	7a, 7b

**Notes:**

\* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1. Three-state is defined as a change from steady-state output.
2. Guaranteed by design neither tested or characterized.



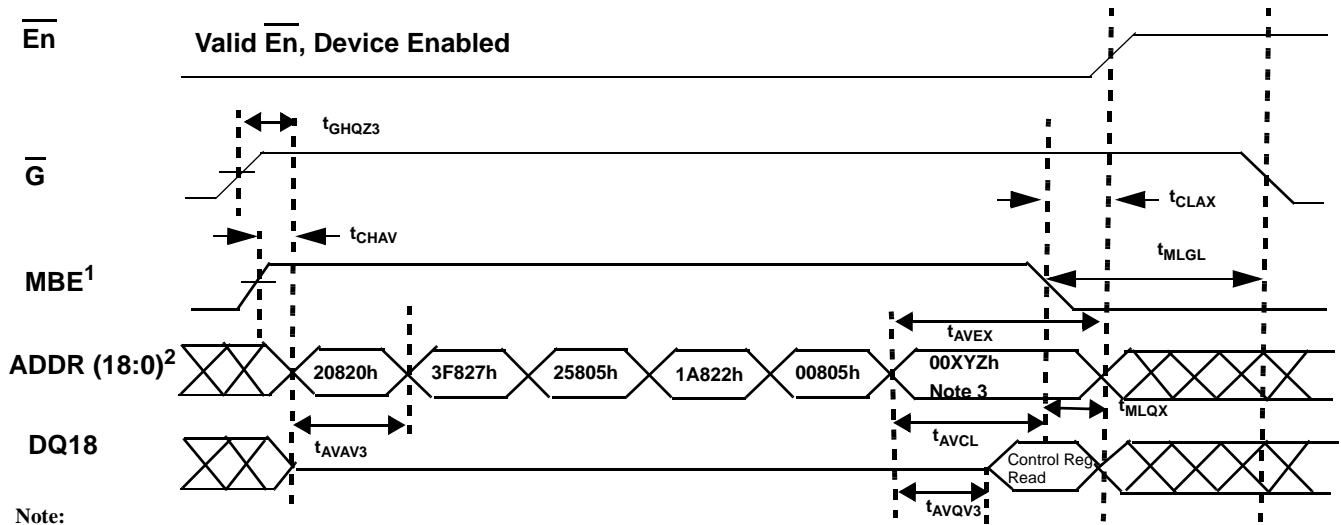
**Note:**

1. MBE is driven high by the user.
2. Device must see a transition to address 70000h coincident with or subsequent to MBE assertion.
3. Lower 10 bits of the last address are used to read or configure the control register (ref Control Register Write/Read Cycles page 9 and Table 5).

**Assumptions:**

1. SCRUB ≥ V<sub>OH</sub> before the start of the configuration cycle. Ignore SCRUB during configuration cycle.

**Figure 7a. Odd Die Numbers (E1, E3, E5, E7 Chip Enables) EDAC Control Register Cycle**



**Note:**

1. MBE is driven high by the user.
2. Device must see a transition to address 20820h coincident with or subsequent to MBD assertion.
3. Bits A2 and A1 are used to read or configure the control register (ref Control Register Write/Read Cycles page 9 and Table 6).

**Assumptions:**

1.  $SCRUB \geq V_{OH}$  before the start of the configuration cycle. Ignore  $\overline{SCRUB}$  during configuration cycle.

**Figure 7b. Even Die Numbers ( $\overline{E2}$ ,  $\overline{E4}$ ,  $\overline{E6}$ ,  $\overline{E8}$  Chip Enables) EDAC Control Register Cycle**

**MASTER MODE AC CHARACTERISTICS (Pre and Post-Radiation)\***

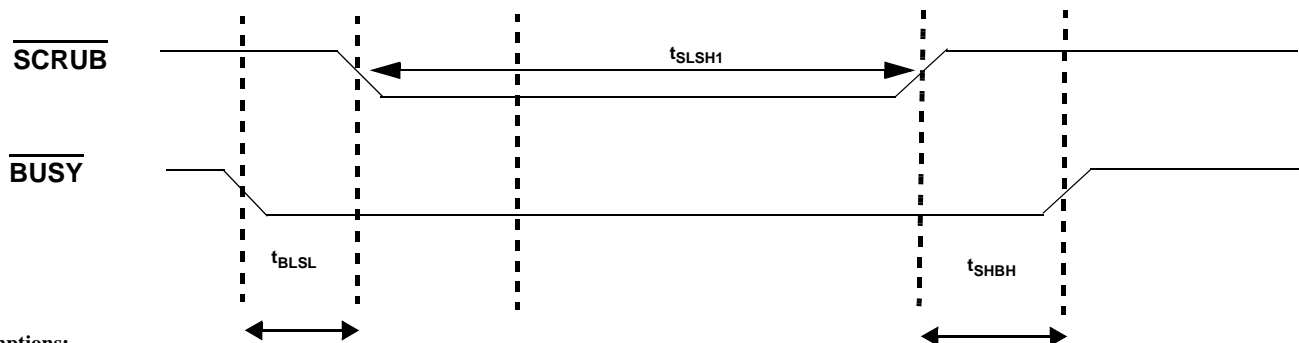
V<sub>DD1</sub> = 1.7V to 2.0V, V<sub>DD2</sub> = 2.3V to 3.6V); Unless otherwise noted, T<sub>c</sub> is per the temperature range ordered

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE
t <sub>BLSL</sub> <sup>1</sup>	User Programmable - $\overline{\text{BUSY}}$ low to $\overline{\text{SCRUB}}$	50*n	(90*n)+1	ns	7c
t <sub>SLSH1</sub>	$\overline{\text{SCRUB}}$ low to $\overline{\text{SCRUB}}$ high	200	350	ns	7c
t <sub>SHBH</sub>	$\overline{\text{SCRUB}}$ high to $\overline{\text{BUSY}}$ high	50	85	ns	7c
t <sub>SCRT</sub> <sup>2</sup>	Scrub Rate Period	2 <sup>n</sup> *50+200	2 <sup>n</sup> *90+350	ns	7c

**Notes:**

\* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1. See Table 5 for User Programmable information. The value "n" is decimal equivalent of hexadecimal value 0x0 through 0xF programmed into control register address bits A<sub>4</sub>-A<sub>7</sub> by user. Default value "n" = 10.
2. See Table 5 for User Programmable information. The value "n" is decimal equivalent of hexadecimal value 0x3 through 0xF programmed into control register address bits A<sub>0</sub>-A<sub>3</sub>. Default value is "n" = 7.



**Assumptions:**

1. The conditions pertain to both a Read or Write.

**Figure 7c. Master Mode Scrub Cycle**

**SLAVE MODE AC CHARACTERISTICS (Pre and Post-Radiation)\***

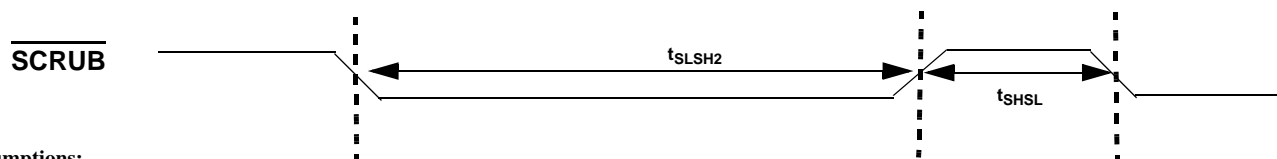
V<sub>DD1</sub> = 1.7V to 1.9V, V<sub>DD2</sub> = 2.3V to 3.6V) Unless otherwise noted, T<sub>c</sub> is per the temperature range ordered

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE
t <sub>SLSH2</sub>	$\overline{\text{SCRUB}}$ low to $\overline{\text{SCRUB}}$ high (slave)	200		ns	7d
t <sub>SHSL</sub> <sup>1</sup>	$\overline{\text{SCRUB}}$ high to $\overline{\text{SCRUB}}$ low (slave)	400		ns	7d

**Notes:**

\* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

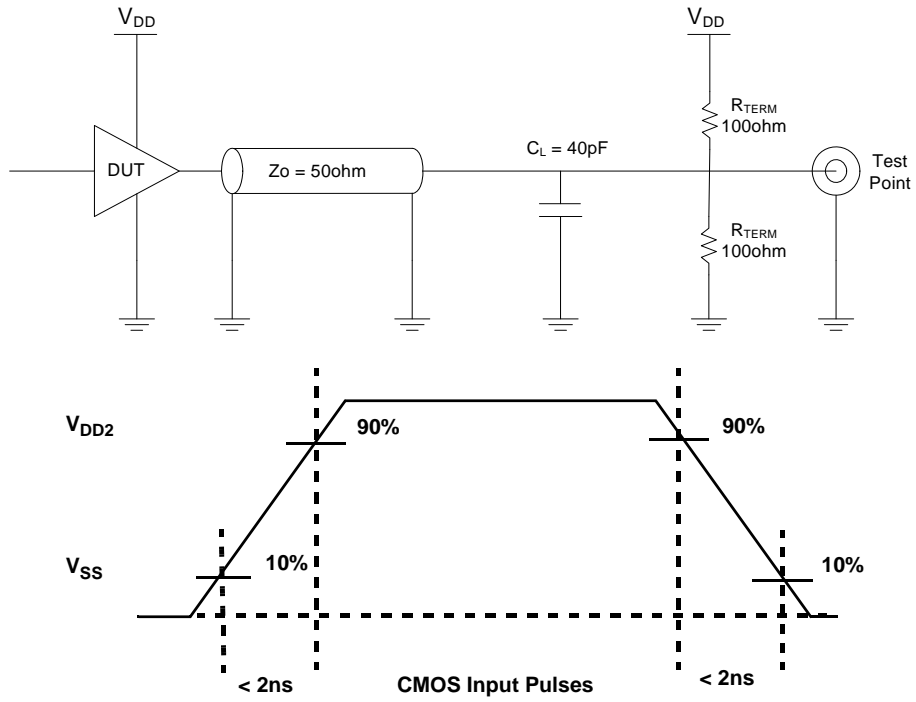
1. Guaranteed by design, neither tested nor characterized.



**Assumptions:**

1. The conditions pertain to both a Read or Write.

**Figure 7d. Slave Mode Scrub Cycle**



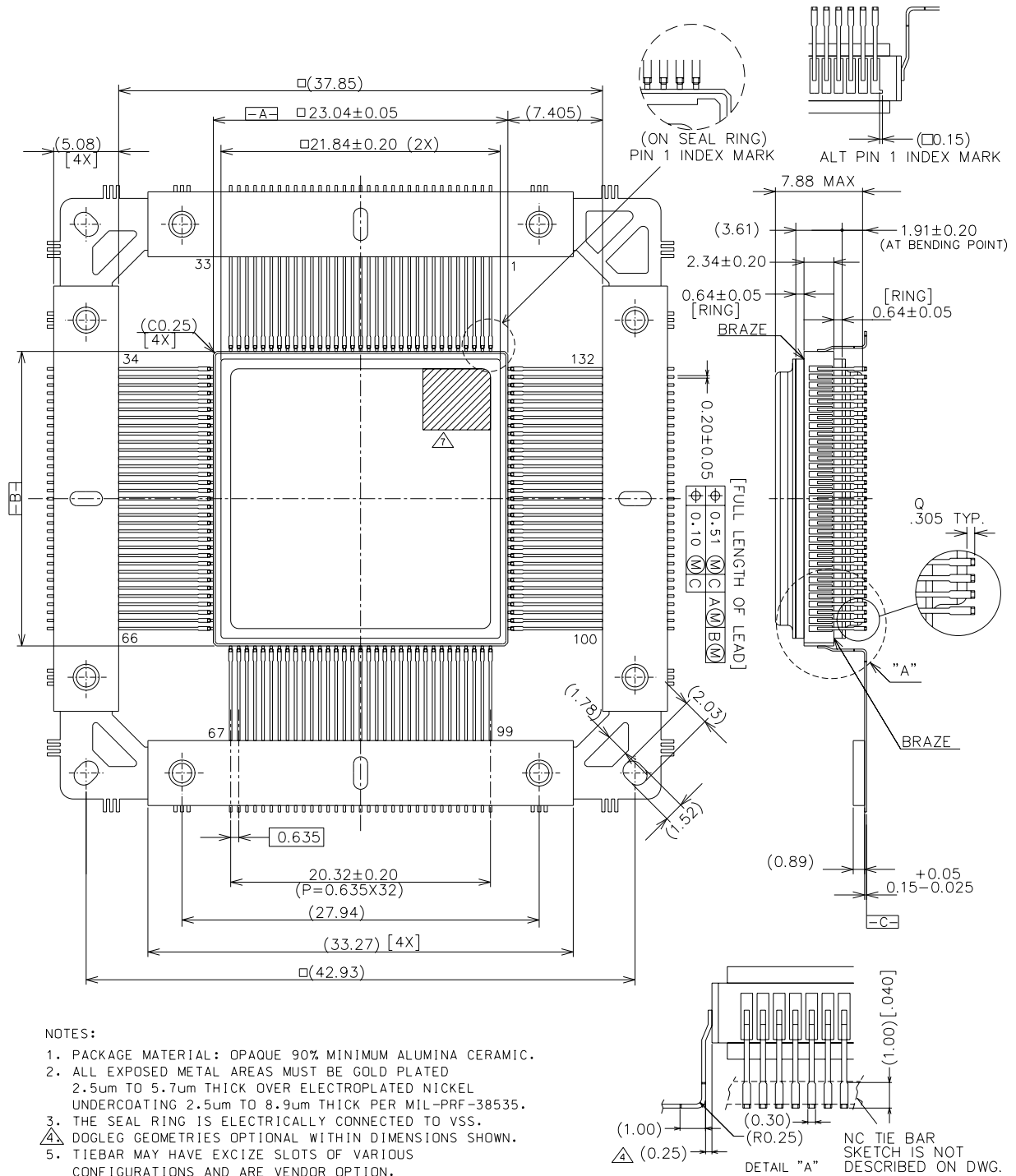
**Notes:**

1. Measurement of data output occurs at the low to high or high to low transition mid-point (i.e., CMOS input =  $V_{DD2}/2$ )

**Figure 8. AC Test Loads and Input Waveforms**



**PACKAGING**

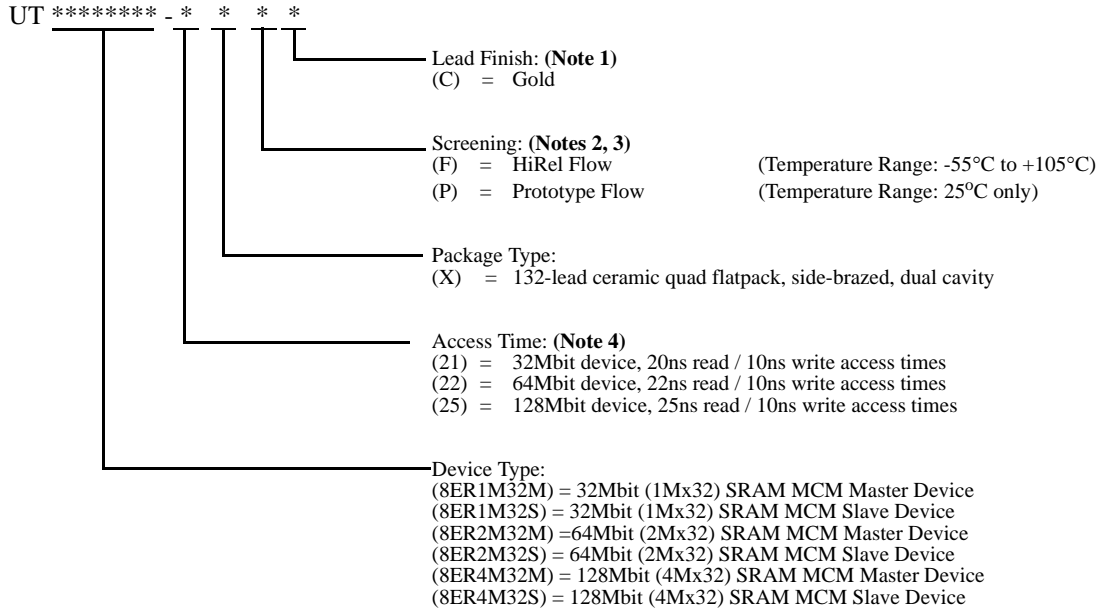


**Figure 9. 132-Lead Side-Brazed Dual Cavity Ceramic Quad Flatpack**

355/A

**ORDERING INFORMATION**

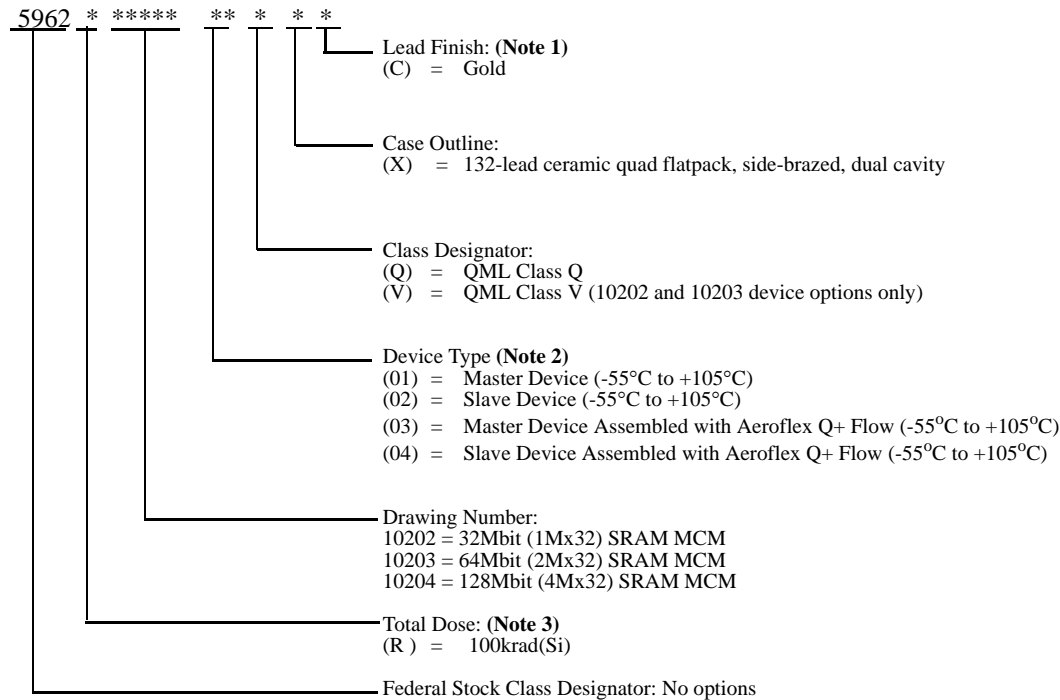
**32Mbit (1Mx32) SRAM MCM**  
**64Mbit (2Mx32) SRAM MCM**  
**128Mbit (4Mx32) SRAM MCM**



**Notes:**

1. Lead finish is "C" (Gold) only.
2. Prototype Flow per Aeroflex Manufacturing Flows Document. Devices are tested at 25°C only. Lead finish is GOLD "C" only. Radiation is neither tested nor guaranteed.
3. HiRel flow per Aeroflex Manufacturing Flows Document. Radiation is neither tested nor guaranteed.
4. Device option (21) is applicable to 32Mbit device types only. Option (22) is applicable to 64Mbit device types only. Option (25) is applicable to 128Mbit device types only.

**32Mbit (1Mx32) SRAM MCM:SMD**  
**64Mbit (2Mx32) SRAM MCM:SMD**  
**128Mbit (4Mx32) SRAM MCM:SMD**



**Notes:**

1. Lead finish is "C" (Gold) only.
2. Aeroflex's Q+assembly flow, as defined in section 4.2.2.d of the SMD, provides QML-Q product through the SMD that is manufactured with Aeroflex's standard QML-V flow.
3. TID tolerance guarantee of 1E5 is tested in accordance with MIL-STD-883 Test Method 1019 (condition A and section 3.11.2) resulting in an effective dose rate of 1 rad(Si)/sec.

## ***Aeroflex Colorado Springs - Datasheet Definition***

**Advanced Datasheet - Product In Development**

**Preliminary Datasheet - Shipping Prototype**

**Datasheet - Shipping QML & Reduced Hi-Rel**

**This product is controlled for export under the Export Administration Regulations (EAR), 15 CFR Parts 730-774. A license from the Department of Commerce may be required prior to the export of this product from the United States.**

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**DATA SHEET REVISION HISTORY**

<b>REV</b>	<b>Revision Date</b>	<b>Description of Change</b>	<b>Page(s)</b>	<b>Author</b>
1.0.0	6/15	Added new datasheet format	All	Leslie
2.0.0	12/15	Added new Table 1, edited Master and Slave Mode AC Characteristics, and updated export disclaimer	3, 22, 28	Leslie

## Low Power SRAM Read Operations

**Table 1: Cross Reference of Applicable Products**

Product Name:	Manufacturer Part Number	SMD #	Device Type	Internal PIC Number:*
4M Asynchronous SRAM	UT8R128K32	5962-03236	01 & 02	WC03
4M Asynchronous SRAM	UT8R512K8	5962-03235	01 & 02	WC01
16M Asynchronous SRAM	UT8CR512K32	5962-04227	01 & 02	MQ08
16M Asynchronous SRAM	UT8ER512K32	5962-06261	05 & 06	WC04/05
4M Asynchronous SRAM	UT8Q512E	5962-99607	05 & 06	WJ02
4M Asynchronous SRAM	UT9Q512E	5962-00536	05 & 06	WJ01
16M Asynchronous SRAM	UT8Q512K32E	5962-01533	02 & 03	QS04
16M Asynchronous SRAM	UT9Q512K32E	5962-01511	02 & 03	QS03
32M Asynchronous SRAM	UT8ER1M32	5962-10202	01 - 04	QS16/17
64M Asynchronous SRAM	UT8ER2M32	5962-10203	01 - 04	QS09/10
128M Asynchronous SRAM	UT8ER4M32	5962-10204	01 - 04	QS11/12
40M Asynchronous SRAM	UT8R1M39	5962-10205	01 & 02	QS13
80M Asynchronous SRAM	UT8R2M39	5962-10206	01 & 02	QS14
160M Asynchronous SRAM	UT8R4M39	5962-10207	01 & 02	QS15

\* PIC = Aeroflex's internal Product Identification Code

### **1.0 Overview**

The purpose of this application note is to discuss the Aeroflex SRAMs low power read architecture and to inform users of the affects associated with the low power read operations.

### **2.0 Low Power Read Architecture**

The aforementioned Aeroflex designed SRAMs all employ an architecture which reduces power consumption during read accesses. The architecture internally senses data only when new data is requested. A request for new data occurs anytime the chip enable device pin is asserted, or any of the device address inputs transition states while the chip enable is asserted. A trigger is generated and sent to the sensing circuit anytime a request for new data is observed. Since several triggers could occur simultaneously, these triggers are wire-ORed to result in a single sense amplifier activity for the read request. This design method results in less power consumption than designs that continually sense data. Aeroflex's low power SRAMs listed above activate the sensing circuit for approximately 5ns whenever and access is requested, thereby, significantly reducing active power.

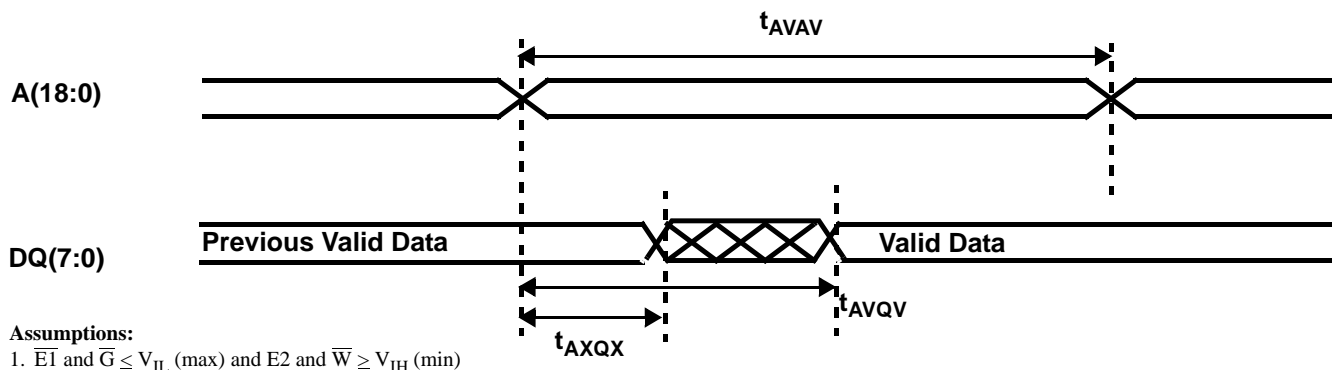
## 2.1 The SRAM Read Cycles.

The data sheets for all the devices noted in Table #1 discuss three methods for performing a read operation. The two most common methods for reading data are an Address Access and a Chip Enabled-Controlled Access. The third access discussed is the Output Enable-Controlled Access. The sequence at which control lines and address inputs are toggled determines which cycle is considered relevant. As discussed in section 2.0, an assertion of chip enable or any address transition while chip enable is asserted, initiates a read cycle. If the device chip enable is asserted prior to any address input transitions, then the read access is considered an Address Access. By keeping the device enabled and repeatedly switching address locations, the user retrieves all data of interest. A Chip Enable-Controlled Access occurs when the address signals are stable prior to asserting the chip enable. The Output Enabled-Controlled Access requires that either an Address Access or Chip Enable-Controlled Access has already been performed and the data is waiting for the Output Enable pin to assert, driving data to the device I/O pins.

The subsequent read cycle verbiage and diagrams are based on the Aeroflex UT8R512K8 data sheet. The number of control, input, and I/O pins will vary across the products listed in Table 1. The basic design family functionality for read operations is common among all the devices.

### 2.1.0 Address Access Read Cycle

The Address Access is initiated by a change in address inputs while the chip is enabled with  $\overline{G}$  asserted and  $\overline{W}$  deasserted. Valid data appears on data outputs DQ(7:0) after the specified  $t_{AVQV}$  is satisfied. Outputs remain active throughout the entire cycle. As long as chip enable and output enable are active, the address inputs may change at a rate equal to the minimum read cycle time ( $t_{AVAV}$ ).

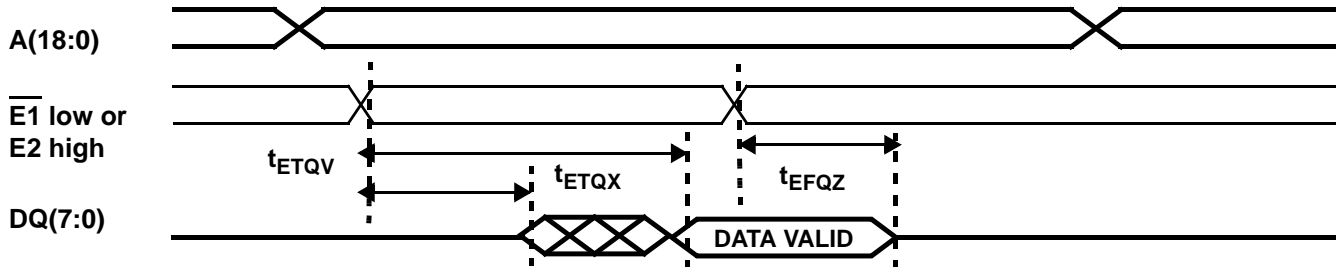


Note: No time references are relevant with respect to Chip Enable(s). Chip Enable(s) is assumed to be asserted.

SRAM Read Cycle 1: Address Access

## 2.1.1 Chip Enable-Controlled Read Cycle

The Chip Enable-controlled Access is initiated by  $\overline{E1}$  and E2 going active while  $\overline{G}$  remains asserted,  $\overline{W}$  remains deasserted, and the addresses remain stable for the entire cycle. After the specified  $t_{ETQV}$  is satisfied, the eight-bit word addressed by A(18:0) is accessed and appears at the data outputs DQ(7:0).



**Assumptions:**

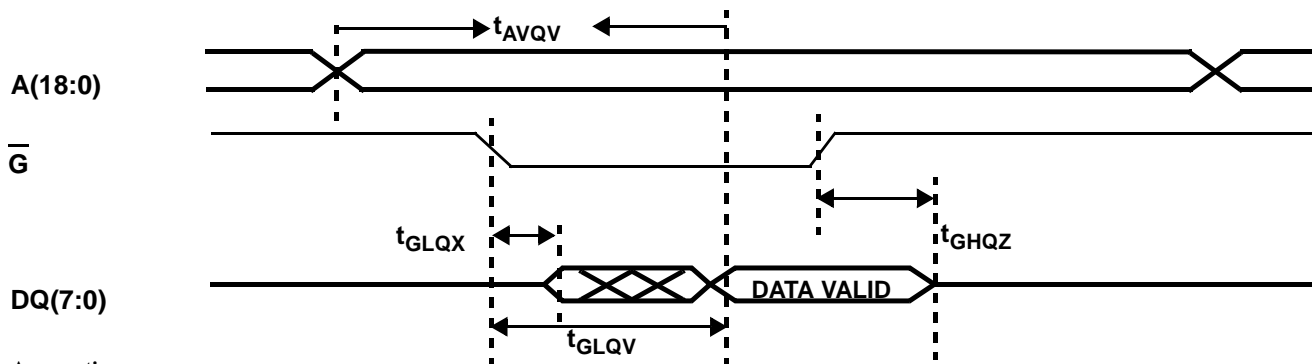
1.  $\overline{G} \leq V_{IL}(\text{max})$  and  $\overline{W} \geq V_{IH}(\text{min})$

Note: No specification is given for address set-up time with respect to chip enable assertion. The read cycle description states that addresses are to remain stable for the entire cycle. Address set-up time relative to chip enable is assumed to be 0ns minimum.

### SRAM Read Cycle 2: Chip Enable Access

## 2.1.1 Output Enabled-Controlled Read Cycle

The Output Enable-controlled Access is initiated by  $\overline{G}$  going active while  $\overline{E1}$  and E2 are asserted,  $\overline{W}$  is deasserted, and the addresses are stable. Read access time is  $t_{GLQV}$  unless  $t_{AVQV}$  or  $t_{ETQV}$  have not been satisfied.



**Assumptions:**

1.  $\overline{E1} \leq V_{IL}(\text{max})$ ,  $E2 >$  and  $\overline{W} \geq V_{IH}(\text{min})$

### SRAM Read Cycle 3: Output Enable Access

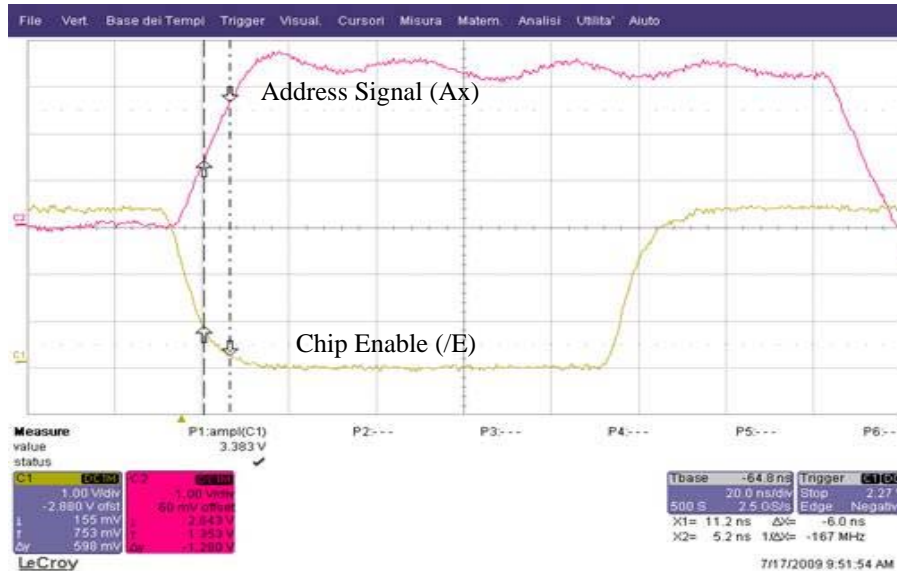
## 3.0 Low Power Read Architecture Timing Consideration

The low power read architecture employed by Aeroflex designed SRAMs results in significant power reduction, especially in applications with longer than minimum read cycle times. However, this type of architecture is responsive to excessive input signal skew when device addressing and chip enable assertion occur simultaneously. Signal skew of greater than 4-5ns between all of the read triggering activities is sufficient to start another read cycle.



### 3.1 Simultaneous Control and Address Switching

Simultaneous switching of controls and address pins, alone, is not a problem; excessive skew between them is the concern. Consider the application where several SRAM devices are connected to the same memory bus. The address bus is commonly connected to all the devices, but the chip enable pin is singularly connected to each individual SRAM. This configuration results in a loading difference between the address inputs and the chip enable. This lightly loaded chip enable propagates to the memory more quickly than the heavily loaded address lines. The oscilloscope capture of Figure #1 is the actual timing of an application which had intermittent data errors due to address transitions lagging chip enable.



- Timing shown from VIL (yellow trace /CS) and VIH (pink for address signal) as  $\Delta X = 6\text{ns}$ . Even at actual internal gate switching point ( $\sim V_{DD}/2$ ), the skew is still around 6ns.

Figure #1 SRAM Signal Capture

The signal transitions in the scope plot of Figure #1 appear to be fairly coincidental. A closer look however, reveals the chip enable signal actually starts and reaches  $V_{IL}$  approximately 6ns before the address signal reaches  $V_{IH}$ . Even at one half  $V_{DD}$  (closer to actual logical gate switching of the inputs), the delta in signal times is still approximately 6ns.

Simultaneous switching of controls and address inputs is not recommended for a couple of reasons. The first is the previously described signal skew sensitivity between controls and/or address inputs. The second reason is that activating all the controls and address inputs simultaneously results in peak instantaneous current consumption. This condition causes maximum strain to the power decoupling. Chip Enable activates address decoding circuits, address switching introduces input buffer switching current, and output enable assertion turns on all the device output drivers. Performing all three simultaneously results in worst case transient current demand by the memory.

#### 3.1.0 Technical Overview of Skew Sensitivity

Recall from section 2.0 that any activity requesting new data causes a read trigger. The triggers are wire-ORed together. In order to meet the faster access times demanded by today's applications, the ORed trigger only exists during the first 4-5ns of the read cycle. Since the slowest of the address transitions occurs more than 5ns after the initiation of the read activity, a second read activity is initiated. The sensing circuit does not have time to normalize before the second read activity has started. For this reason a Chip Enable-Controlled read cycle requires that address inputs remain stable for the entire cycle. Infrequent and random sensing errors can result if the bit columns are continually pulled to one state then quickly requested to sense the opposite state. Another effect of the low power read architecture that differs from previous generation designs (those that continually sense for data) is that the bit line will not be sensed again until another read triggering event occurs. If another read trigger event (chip enable assertion and/or address change) does not occur for a particular address, the incorrect data remains at the outputs.

## **4.0 Summary and Conclusion**

The Aeroflex SRAMs in Table #1 all employ a low power consumption read architecture. Power is conserved by sensing data only when new data is requested. A request occurs anytime chip enable is asserted or any address input signal transitions while chip enable is asserted. The data sheets for the SRAMs listed in Table #1 do not explicitly define the case of simultaneous switching of address and control signals during read operations. Data sheet read cycle descriptions indicate that control inputs are established prior to address changes, and address inputs are stable prior to control assertions. Simultaneous switching of addresses and controls is tolerable, when the skew between all input signals is  $< 4\text{ns}$ . For designs that must employ the simultaneous activation of address and control signals, two important issues should be considered by the designer. The first is the input signal skew sensitivity of the low power read architecture discussed by this application note. The second is the instantaneous current consumption that results from simultaneous access methods. Aeroflex recommends the use of only one read access method at a time. If multiple read accesses (simultaneous chip enable assertion and address switching) cannot be avoided, then Aeroflex recommends that the chip enable signal be delayed until all addresses have completed transitions.