Standard Products

UT7R2XLR816 Clock Network Manager

Datasheet
June 2017

The most important thing we build is trust

FEATURES:

- +3.3V Core Power Supply
- Independent power supply for each clock bank
  - Power supply range from +2.25V to +3.6V
- 8 Output clock banks with flexible I/O signaling
  - Up to 16 LVCMOS3.3 outputs with 12mA slew-rate limited, break-before-make, buffers, or
  - Up to 16 LVCMOS2.5 outputs with 8mA slew-rate limited, break-before-make, buffers, or
  - Up to 8 standard drive LVDS outputs
- Input clock multiplication of any integer from 1 - 32
- PLL Operation
  - Low frequency range: 24MHz to 50MHz
  - Mid frequency range: 48MHz to 100MHz
  - High frequency range: 96MHz to 200MHz
- Input reference clock signaling and control:
  - LVCMOS3.3/LVTTL (Cold-Spared), LVDS (Cold-Spared), & Parallel Resonant Quartz Crystal
  - Reference input divide-by-1 or divide-by-2
  - Input frequency range from 2MHz to 200MHz
- Dedicated feedback Input/Output module
  - Independent feedback power supply (+3.0V to +3.6V)
  - 1-to-32 divider options with/without inverting
  - Phase control -6, -4, -3, -2, -1, 0, 1, 2, 3, 4, 6 tU
  - FB_IN: Not affected by RST/DIV state
  - FB_OUT = LOW when RST/DIV=LOW (RESET)
  - No Synchronous Output Enable (sOE) control in order to maintain PLL lock
- Output clock bank signaling and control:
  - Output frequency range from 750KHz to 200MHz
  - 1-to-32 divider options with/without inverting
  - Odd bank phase control -4, -3, -2, -1, 0, 1, 2, 3, 4 tU
  - Even bank phase control -6, -4, -2, -1, 0, 1, 2, 4, 6 tU
  - Disable HIGH, LOW, or HIGH-Z (See Table 1, page 6)
  - Synchronous Output Enable (sOE) control
  - Outputs (0-7)Q0, 1 = HIGH-Z/Tri-state when RST/DIV= LOW (RESET)
- Guaranteed reference input to output edge synchronization
- Low inherent output bank skew (e.g. SKEW = 0*tU)
  - < 50ps intrabank skew (typical)
  - < 100ps interbank skew without dividing or inverting (typ)
  - < 250ps interbank skew across divided or inverted banks (typ)
- Power dissipation can be reduced by powering down unused output banks (See Note 2, page 37)
- Temperature range:
  - HiRel: -55°C to +125°C
- Operational environment:
  - Total-dose: 100 krad (Si)
  - SEL Immune to a LET of 109 MeV-cm^2/mg
  - SEU Immune to a LET of 109 MeV-cm^2/mg
- Packaging options (1.27mm pitch, 17mm sq. body):
  - 168-CLGA
  - 168-CBGA
  - 168-CCGA
- Standard Microcircuit Drawing 5962-08243
  - QML Q and Q+
- Applications
  - High altitude avionics
  - X-ray Cargo Scanners
  - Test and Measurement
  - Networking, telecommunications and mass storage

INTRODUCTION:

The UT7R2XLR816 is a low voltage, low power, clock network manager. The device features 16-outputs in 8 banks of 2. Independent power supplies for each bank (+2.25V to +3.6V) give the user great flexibility in multi- voltage systems. Outputs can be configured as LVCMOS (2.5V/8mA or 3.3V/12mA) or standard LVDS pairs. Independent output bank division and phase skewing empower the system designer to optimize output phase and frequency relationships throughout a clock network.

The skew controls enable outputs to lead or lag the reference clock while the ternary output divider control can divide the PLL oscillator frequency by any integer from 1to 32 before driving the clock out of the desired bank. Regardless of output divider settings, input and output clock edges are synchronized at start-up and whenever the device is removed from power down mode. Power down mode is controlled by the RST/DIV ternany input which also controls input division of the reference clock. Time units for skew control (t_U) are 22.5° of the clock cycle for low and mid frequency oscillators and 45° of the clock cycle for the high frequency oscillator.

Slew rate optimization of outputs is determined by the PLL oscillator range selected and thus is controlled by the FREQ_SEL input. Output rise times decrease as higher frequency range oscillators are selected. The input reference clock can be LVCMOS/LVTTL/ LVDS or a quartz crystal. The LVCMOS/LVTTL and LVDS inputs are cold-spared. Input reference frequencies can range from 2MHz to 200MHz. Using the $\overline{\text{RST}}$/DIV pin and FB_DS[3:0] feedback divider settings for the reference clock can be multiplied by 0.5x-32x in steps of 0.5 through a multiplication factor of 16 and integer steps for multiplication factors 17 through 32.

To provide further clock network optimization, the feedback output bank includes independent skew and division control.
PLL lock is identified by the active high LOCK signal. LOCK will only become true when the REFERENCE and FB_IN clocks are stable and aligned to within $t_{LOCKRES}$, which is variable based on the state of the FREQ_SEL pin. At all other times, LOCK will remain LOW.

Clock outputs are deterministic in that if either the reference input clock or feedback clock are absent, the outputs will oscillate at a frequency near the midpoint of the selected PLL operating range.
Test modes are available for user diagnostics. The TEST ternary input enables the test modes. When TEST is low, normal operation occurs. Floating the TEST pin to a mid-range value disables the PLL oscillators and drives the clock output banks with the REF clock input. Setting TEST high disables the PLL oscillators and drives the clock output banks with the FB_IN input.

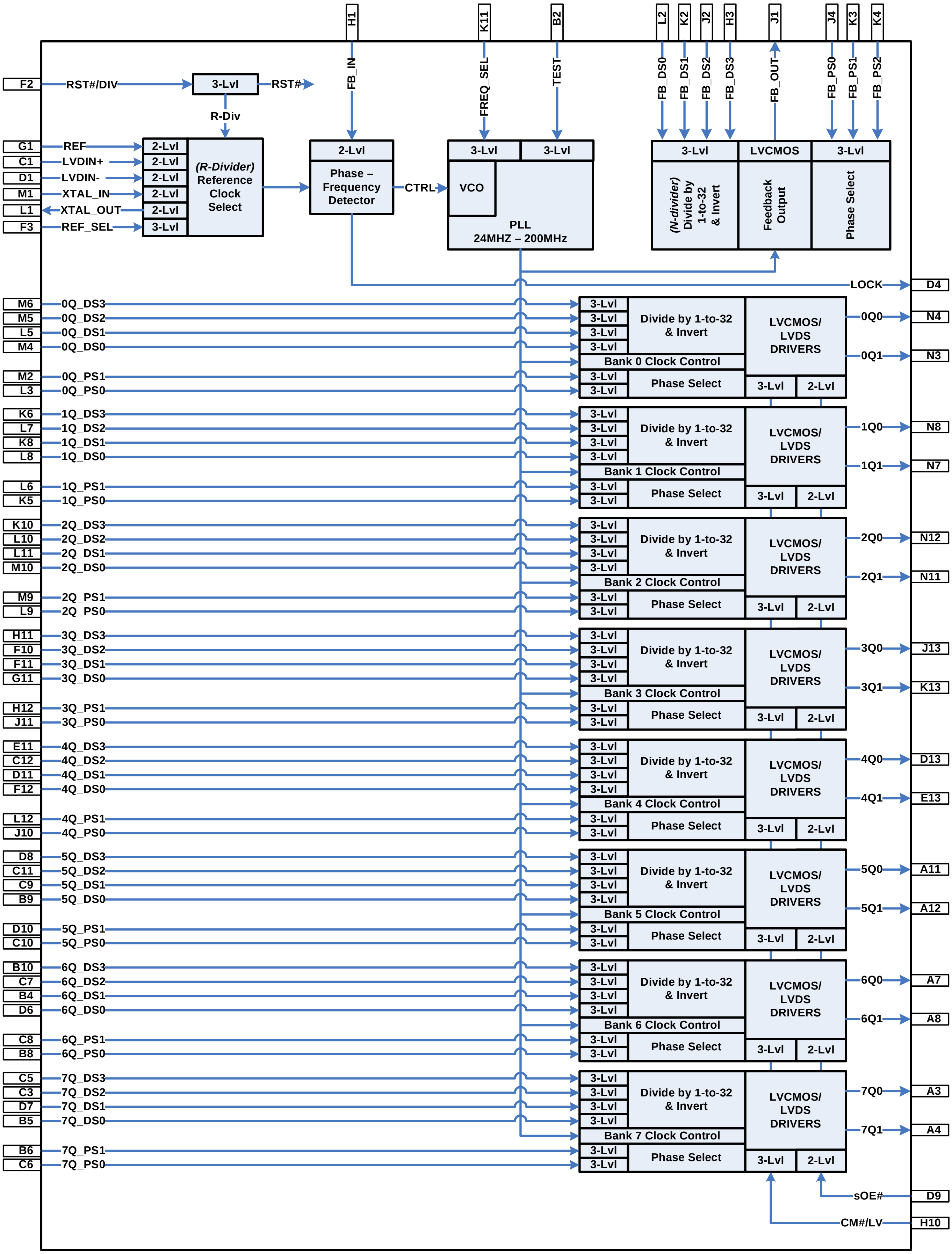

Figure 1. UT7R2XLR816 Block Diagram

1.0 Functional Description

The UT7R2XLR816, clock network manager, has an array of special features designed to overcome many of the clock management and clock distribution challenges common in today's high-performance electronic systems. This section of the datasheet provides an overview of the primary features within and is intended to acquaint the designer with their basic capabilities.

Although discussed in more detail below, the user should understand that many features within the UT7R2XLR816 are selected by ternary control signals. These ternary controls recognize three separate logic levels on a single pin. The L(ow) state means that the control input pin is driven below the V_{ILL} level specified in the DC electrical table of this datasheet. Conversely, a H(igh) means that the control input is driven above the V_{IHH} voltage described in the DC electrical table. While a M(id) state requires that the input pin be floated, allowing the internal resistor divider network to place the pin into a level compliant with the V_{IMM} voltage listed in the DC electrical table, or externally driven/biased to the V_{IMM} level.

1.1 Reference Clocks

The UT7R2XLR816 is capable of receiving its reference clock from one of three sources. The REF input allows for a single ended, LVTTL/LVCMOS clock source. The LVDIN+ and LVDIN- pins combine to receive an LVDS reference clock. The LVDIN+ should be driven by the positive half of the LVDS clock signal while the LVDIN- should be driven by the negative half of the LVDS clock signal. A 100Ω terminating resistor should be connected directly between the LVDIN+ and LVDIN- terminals. Finally, the XTAL_IN and XTAL_OUT terminals provide for a quartz crystal resonator reference clock input. The XTAL_IN pin is the input to the on-chip pierce oscillator and should be connected directly to one side of an external quartz crystal that is tuned to operate in the parallel resonance mode. The XTAL_OUT pin drives out the 180° phase shifted version of the reference clock received on XTAL_IN. The XTAL_OUT pin should drive the other end of the external quartz crystal resonator circuit. Reference figure 3 for an example quartz crystal oscillator circuit.

The REF, LVDIN+ and LVDIN- inputs are cold-spared. The cold-sparing capability of these reference pins make them ideal for receiving an off-board clock source that may be active while the UT7R2XLR816 is unpowered.

The UT7R2XLR816 provides a ternary reference select pin (REF_SEL) that is used to control which of the three available clock sources the UT7R2XLR816 will use as its timing reference. Since REF_SEL ensures that only one reference source can drive the internal circuitry of the UT7R2XLR816 the remaining two clock sources may be driven simultaneously allowing the REF_SEL pin to select between these reference sources. As mentioned above, REF_SEL is a ternary, or three level input. Setting REF_SEL L(ow) selects the XTAL_IN/XTAL_OUT crystal resonator source. Placing REF_SEL into a M(id) level (left floating), sets the REF input as the UT7R2XLR816 reference clock source. Finally, driving REF_SEL H(igh), enables the LVDS (LVDIN+/LVDIN-) clock source. These available REF_SEL configurations are shown in figures 2, 3 and 4.

1.2 Feedback Clock

The UT7R2XLR816 contains a dedicated feedback I/O module that is completely separate from the eight (8) output clock banks. The FB_IN feedback input can be driven directly from the FB_OUT pin, or from a digital circuit having the FB_OUT pin as its source.

The FB_IN signal connects to the internal Phase-Frequency Detector (PFD), which compares the FB_IN signal with the clock reference source as selected by the REF_SEL control. Phase shifts associated with board trace delays from routing, in-line circuitry, or intentional phase skewing within the feedback path are adjusted by the PFD to advance or delay the Phase-Locked Loop (PLL), as necessary, to ensure that the clock arriving at FB_IN is phase aligned with the selected reference clock source.

The FB_OUT is an LVCMOS3 output signal driven by the PLL. As discussed in Tables 1 and 2, the frequency and phase of the FB_OUT signal may be adjusted by the FB_DS[3:0] output divider settings and the FB_PS[2:0] phase selection settings, respectively. Both pin groups, FB_DS[3:0] and FB_PS[2:0], are ternary inputs. The FB_DS[3:0] settings are used to multiply the frequency of the internal PLL by dividing the frequency of the FB_OUT signal.

FB_OUT may be divided by any integer from 1 to 32, as-well-as inverted following the division operation. Inversion provides a 180° phase shift of the PLL from the incoming reference source, effectively synchronizing the PLL to the opposite edge of the reference clock. To ensure stable locking of the PLL and to free the output clock banks to drive the system clock, FB_OUT should always be used as the originating clock source for the FB_IN pin.

The FB_PS[2:0] feedback phase selection pins allow the FB_OUT signal to be phase shifted by -6, -4, -3, -2, -1, 0, 1, 2, 3, 4, or 6 tu (time units). The value of tu is determined by the FREQ_SEL setting and the PLL's operating frequency. Examples of tu calculation are shown in Equation 1 and Table 5. Phase shifting FB_OUT has the effect of advancing or delaying the PLL and, by extension, the nominal phase of all output clock banks. A positive phase shift (i.e. delay) in FB_OUT advances the PLL and clock output banks so they lead the reference clock by the same phase shift amount. Conversely, a negative shift (i.e. advancement) of FB_OUT causes the PLL and output clock banks to lag the reference clock source by the same amount of phase shift.

1.3 Phase-Locked Loop (PLL) and Frequency Generation

The UT7R2XLR816's PLL circuitry consists of the previously mentioned reference and feedback input clock sources, a Phase–Frequency Detector (PFD), and a Voltage-Controlled Oscillator (VCO). The voltage controlled oscillator consists of three separate oscillators that are optimized to run in three specific frequency bands. The ternary FREQ_SEL input is used to select the appropriate VCO based upon the nominal PLL frequency required by the application. The nominal PLL frequency range selected by FREQ_SEL are 24 – 50MHz (FREQ_SEL=Low), 48 – 100MHz (FREQ_SEL=Mid) and 96 – 200MHz (FREQ_SEL=High).

The UT7R2XLR816 includes an internal reset signal to ensure that the selected VCO starts-up and the PLL establishes lock with the stable reference clock sources whenever power is applied to the device, or the device is dynamically reconfigured to select a different VCO. However, Aeroflex recommends that dynamic reconfiguration be performed while the device is held in RESET (e.g. $\overline{\text{RST}}$/DIV=Low) to ensure a smooth re-start and avoid uncontrolled behavior from the device during the reconfiguration process.

An additional start-up feature provided by the UT7R2XLR816 is the inclusion of a PLL pre-charge circuit that places the selected VCO into a mid-band frequency of operation in the event that either one, or both, of the reference and feedback clocks are removed or drop to a frequency below f_{REFDET}. The intent of this feature is to ensure that the PLL demonstrates deterministic behavior if the device is out of reset and the PFD does not receive valid, stable, input clocks. By controlling the active VCO when the PFD does not have a valid set of input clocks to compare ensures that any active output clock bank oscillates at a manageable frequency for downstream electronics. It is also recommended that the $\overline{\text{sOE}}$ pin be used in conjunction with the UT7R2XLR816 startup by disabling the output banks until the device has completed its PLL locktime (tLOCK) and the LOCK output is stable high.

When valid, stable, reference and feedback clocks are available to the PFD, it will override the pre-charge circuitry and begin to control the VCO. Although the PFD works to maintain frequency and phase alignment between the reference and FB_IN to an ideal 0ns difference, it will inform the user that the PLL is locked onto the incoming clocks when they are phase aligned to within 2ns (typical) for the low and mid VCO selections, and within 1.5ns (typical) for the high VCO. When this condition is met, the UT7R2XLR816 will drive the LOCK output high, indicating to the system the PLL is locked. When the LOCK pin is LOW, the PLL is not locked and the clock outputs may not be stable or synchronized to the reference clock source. The LOCK will de-assert LOW when the reference clock and the FB_IN are separated by greater than the defined alignments, unless the device is reset.

2.0 DEVICE CONFIGURATION:

Table 1: Output Divider Settings
FB (N-factor) & Bank 0Q through Bank 7Q (M_{nQ}-factor)

DS[3:0]	Output Divider	DS[3:0]	Output Divider	DS[3:0]	Output Divider
LLLL	1	MLLL	28	HLLL	23+INV
LLLM	2	MLLM	29	HLLM	24+INV
LLLH	3	MLLH	30	HLLH	25+INV
LLML	4	MLML	31	HLML	26+INV
LLMM	5	MLMM	32	HLMM	27+INV
LLMH	6	MLMH	1+INV	HLMH	28+INV
LLHL	7	MLHL	2+INV	HLHL	29+INV
LLHM	8	MLHM	3+INV	HLHM	30+INV
LLHH	9	MLHH	4+INV	HLHH	31+INV
LMLL	10	MMLL	5+INV	HMLL	32+INV
LMLM	11	MMLM	6+INV	HMLM	Note 1
LMLH	12	MMLH	7+INV	HMLH	Note 1
LMML	13	MMML	8+INV	HMML	Note 1
LMMM	14	MMMM	9+INV	HMMM	Note 1
LMMH	15	MMMH	10+INV	HMMH	Note 1
LMHL	16	MMHL	11+INV	HMHL	Note 1
LMHM	17	MMHM	12+INV	HMHM	Note 1
LMHH	18	MMHH	13+INV	HMHH	Note 1
LHLL	19	MHLL	14+INV	HHLL	DIS_LO Note 2
LHLM	20	MHLM	15+INV	HHLM	Note 1
LHLH	21	MHLH	16+INV	HHLH	DIS_HI Note 2
LHML	22	MHML	17+INV	HHML	Note 1
LHMM	23	MHMM	18+INV	HHMM	Note 1
LHMH	24	MHMH	19+INV	HHMH	Note 1
LHHL	25	MHHL	20+INV	HHHL	Note 1
LHHM	26	MHHM	21+INV	HHHM	Note 1
LHHH	27	MHHH	22+INV	HHHH	HI-Z Note 2

Notes:
1. These DS[3:0] settings are for engineering modes only and will default to the DS[3:0] = LLLL state when selected by a user.
2. These DS[3:0] settings are not available on the FB_OUT clock. If selected by the user, the FB_OUT clock will default to the DS[3:0] = LLLL state.

Table 2: Feedback Bank or Output Bank Phase Select Setting[1]

FB_PS [2:0]	Skew FB		nQ_PS [1:0]	Skew EVEN Banks	Skew ODD Banks
LLL	$-6t_U$		LL	$-6t_U$	$-4t_U$
LLM	$-4t_U$		LM	$-4t_U$	$-3t_U$
LLH	$-3t_U$		LH	$-2t_U$	$-2t_U$
LML	$-2t_U$		ML	$-1t_U$	$-1t_U$
LMM	$-1t_U$		MM	Zero Skew	Zero Skew
LMH	Zero Skew		MH	$+1t_U$	$+1t_U$
LHL	$+1t_U$		HL	$+2t_U$	$+2t_U$
LHM	$+2t_U$		HM	$+4t_U$	$+3t_U$
LHH	$+3t_U$		HH	$+6t_U$	$+4t_U$
MLL	$+4t_U$				
MLM	$+6t_U$				
MLH	Note 2				
MML	Note 2				
MMM	Note 2				
MMH	Note 2				
MHL	Note 2				
MHM	Note 2				
MHH	Note 2				
HLL	Note 2				
HLM	Note 2				
HLH	Note 2				
HML	Note 2				
HMM	Note 2				
HMH	Note 2				
HHL	Note 2				
HHM	Note 2				
HHH	Note 2				

Notes:
1. Skew accuracy is within +/- 300ps of $n*t_U$ where "n" is the selected number of skew steps.
2. These skew settings are for engineering modes only and will default to the ZERO SKEW state when selected by a user.

Table 3: Calculating Output Frequency Settings [1, 2]

	Output Frequency	
PLL Operating Frequency (f_{PLL})	**FB_OUT**	**nQ[1:0]**
$(N/R) * f_{REFERENCE}$	$(1/N) * f_{PLL}$	$(1/M_{nQ}) * f_{PLL}$

Notes:
1. Reference Table 1 for N-factor and MnQ-factor. Reference RST/DIV pin description for R-factor.
2. The N-factor, R-factor, and Reference frequency should be selected such that the PLL oscillates within a range defined by the Frequency Selection shown in Table 4.

Table 4: Frequency Range Select

FREQ_SEL	Nominal PLL Frequency Range (f_{PLL})
L	24 MHz to 50 MHz
M	48 MHz to 100 MHz
H	96 MHz to 200 MHz

Selectable output skew is in discrete increments of time unit (t_U). The value of t_U is determined by the FREQ_SEL setting and the PLL's operating frequency (f_{PLL}). Use the following equation to calculate the time unit (t_U):

Equation 1. $$t_u = \frac{1}{(f_{PLL} * MF)}$$

The f_{PLL} term, which is calculated with the help of Table 3, must be compatible with the nominal frequency range selected by the FREQ_SEL signal as defined in Table 4. The multiplication factor (MF), also determined by FREQ_SEL, is shown in Table 5. The UT7R2XLR816 output skew steps have a typical accuracy of +/- 300ps of the calculated time unit (t_U).

Table 5: MF Calculation

FREQ_SEL	MF	f_{PLL} examples that result in a t_U of 1.0ns
L	32	31.25 MHz
M	16	62.5 MHz
H	8	125 MHz

2.1 Reference Clock Interface

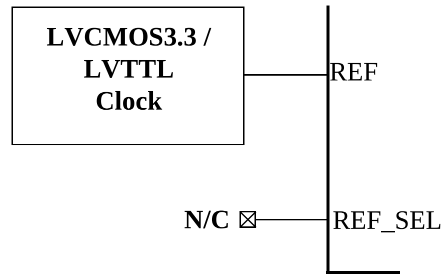

Figure 2. LVCMOS3.3/LVTTL Reference Clock Interface

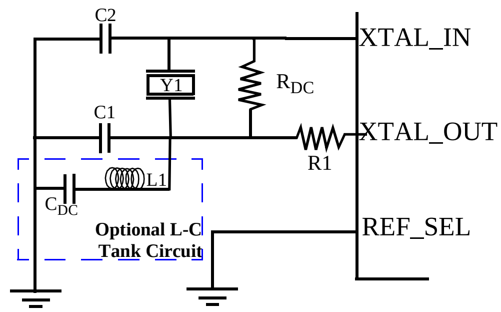

Figure 3. Parallel Resonant Crystal Reference Interface

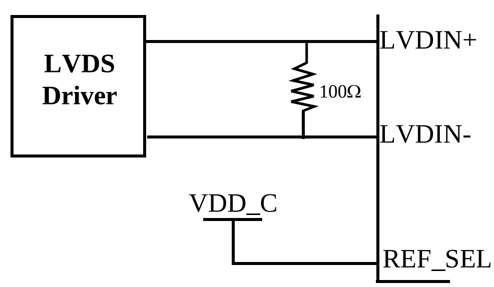

Figure 4. LVDS Reference Clock Interface

3.0 OPERATIONAL ENVIRONMENT

Table 6: Operational Environment Design Specifications

Parameter	Limit	Units
Total Ionizing Dose (TID)	min = none max = 1E5	rads(Si)
Single Event Latchup (SEL) [1, 2]	>109	MeV-cm^2/mg
Onset Single Event Upset (SEU) LET Threshold [3]	>109	MeV-cm^2/mg
Onset Single Event Transient (SET) LET Threshold [4] @ 50 MHz; FREQ_SEL = L @ 24 MHz; FREQ_SEL = L	 >60 >50	MeV-cm^2/mg
Neutron Fluence	1.0E14	n/cm^2

Notes:

1. The UT7R2XLR816 is latchup immune to particle LETs >109 MeV-cm^2/mg.
2. Worst case temperature and voltage of T_C = +125°C, VDD_A/C = 3.6V, V_{DD_nQ} = 3.6V for SEL.
3. Worst case temperature and voltage of T_C = +25°C, VDD_A/C = 3.0V, V_{DD_nQ} = 3.0V for SEU.
4. Worst case temperature and voltage of T_C = +25°C, VDD_A/C = 3.0V, V_{DD_nQ} = 2.25V for SET.

	N	M	L	K	J	H	G	F	E	D	C	B	A
1	VDD_C	XTAL_IN	XTAL_OUT	VSS_C	FB_OUT	FB_IN	REF	VSS_C	VDD_A	LVD IN-	LVD IN+	VDD_C	
2	VSS_0Q	0Q_PS1	FB_DS0	FB_DS1	FB_DS2	VDD_C	VDD_C	RST#/DIV	VDD_A	VDD_C	VSS_C	TEST	VSS_7Q
3	0Q1	VDD_C	0Q_PS0	FB_PS1	VDD_C	FB_DS3	VSS_C	REF_SEL	VSS_A	VDD_C	7Q_DS2	VDD_C	7Q0
4	0Q0	0Q_DS0	VSS_C	FB_PS2	FB_PS0	VSS_C	VDD_C	VDD_C	VSS_C	LOCK	VSS_C	6Q_DS1	7Q1
5	VDD_0Q	0Q_DS2	0Q_DS1	1Q_PS0	VDD_C	VDD_C	VSS_C	VDD_C	VDD_C	VSS_C	7Q_DS3	7Q_DS0	VDD_7Q
6	VSS_1Q	0Q_DS3	1Q_PS1	1Q_DS3	VDD_C	VSS_C	VSS_C	VSS_C	VDD_C	6Q_DS0	7Q_PS0	7Q_PS1	VSS_6Q
7	1Q1	VDD_C	1Q_DS2	VDD_C	VSS_C	VSS_C	VSS_C	VSS_C	VSS_C	7Q_DS1	6Q_DS2	VDD_C	6Q0
8	1Q0	VSS_C	1Q_DS0	1Q_DS1	VDD_C	VSS_C	VSS_C	VSS_C	VSS_C	5Q_DS3	6Q_PS1	6Q_PS0	6Q1
9	VDD_1Q	2Q_PS1	2Q_PS0	VSS_C	VDD_C	VDD_C	VSS_C	VDD_C	VDD_C	sOE#	5Q_DS1	5Q_DS0	VDD_6Q
10	VDD_2Q	2Q_DS0	2Q_DS2	2Q_DS3	4Q_PS0	CM#/LV	VDD_C	3Q_DS2	VDD_C	5Q_PS1	5Q_PS0	6Q_DS3	VDD_5Q
11	2Q1	VSS_C	2Q_DS1	FREQ_SEL	3Q_PS0	3Q_DS3	3Q_DS0	3Q_DS1	4Q_DS3	4Q_DS1	5Q_DS2	VSS_C	5Q0
12	2Q0	VDD_C	4Q_PS1	VDD_C	VSS_C	3Q_PS1	VDD_C	4Q_DS0	VSS_C	VDD_C	4Q_DS2	VDD_C	5Q1
13	VSS_2Q	VDD_C	VSS_3Q	3Q1	3Q0	VDD_3Q	VSS_C	VDD_4Q	4Q1	4Q0	VSS_4Q	VDD_C	VSS_5Q

Figure 5. 168-CLGA Pinout (view looking through top of package)

4.0 PIN DESCRIPTION

168 CLGA Pin No.	Name	I/O	Type	Description
REFERENCE BLOCK				
G1	REF	IN	COLD SPARED LVCMOS or LVTTL	**Digital reference clock input.** This cold spared input should be driven by a single-ended LVTTL/ LVCMOS clock source. Because REF_SEL selects which reference clock drives the PLL, this input may be actively driven when not selected, but it should never be left floating.
M1	XTAL_IN	IN	CRYSTAL	**Quartz crystal resonator reference clock input.** This pin is the input to the on-chip pierce oscillator. This input should be connected to the output of an external quartz crystal that is tuned to operate in the parallel mode of resonance. Because REF_SEL selects which reference clock drives the PLL, this input may be actively driven when not selected, but it should never be left floating.
L1	XTAL_OUT	OUT	CRYSTAL	**Quartz crystal resonator reference clock output.** This pin drives the 180^{o} phase shifted version of the reference signal received on XTAL_IN. This pin should be connected to the input of the external quartz crystal resonator circuit.
C1	LVDIN+	IN	COLD SPARED LVDS	**Positive LVDS reference clock input terminal.** This cold spared input should be driven by the positive half of an LVDS clock signal. A 100Ω terminating resistor should be connected directly between this terminal and its complement LVDIN-. Because REF_SEL selects which reference clock drives the PLL, this input may be actively driven when not selected or left floating in the fail-safe state.
D1	LVDIN-	IN	COLD SPARED LVDS	**Negative LVDS reference clock input terminal.** This cold spared input should be driven by the negative half of an LVDS clock signal. A 100Ω terminating resistor should be connected directly between this terminal and its complement LVDIN+. Because REF_SEL selects which reference clock drives the PLL, this input may be actively driven when not selected or left floating in the fail-safe state.

<table>
<tr><th>168 CLGA
Pin No.</th><th>Name</th><th>I/O</th><th>Type</th><th>Description</th></tr>
<tr><td>F3</td><td>REF_SEL</td><td>IN</td><td>3-LEVEL</td><td>Reference selection input.
This ternary input selects one of the three user reference sources to drive the internal PLL.

Note: The input buffers on the reference sources that are NOT selected by REF_SEL are disabled LOW.

Note: When the device is placed into the reset mode of operation (e.g. $\overline{\text{RST}}$/DIV = LOW), the XTAL_IN/XTAL_OUT buffers will remain enabled if REF_SEL = LOW.

<table>
<tr><th>REF_SEL</th><th>Selected Source</th></tr>
<tr><td>LOW</td><td>XTAL_IN</td></tr>
<tr><td>MID</td><td>REF</td></tr>
<tr><td>HIGH</td><td>LVDIN+, LVDIN-</td></tr>
</table></td></tr>
<tr><td>F2</td><td>$\overline{\text{RST}}$/DIV</td><td>IN</td><td>3-LEVEL</td><td>Reset and reference divider control.
This ternary input operates as a dual function pin that controls the reset operation and selects the input reference divider. When driven HIGH, the selected input reference will directly drive the PLL. Allowing this pin float results in the selected reference source being divided in half before it drives the PLL.

Holding the pin low during power up and reference clock stabilization ensures clean UT7R2XLR816 startup that is independent of the power-up behavior of the reference clock. The pin may also be driven low at any time to force a reset to the PLL and the output divider synchronization.

Note: When the device is placed into the reset mode of operation (e.g. $\overline{\text{RST}}$/DIV = LOW), the XTAL_IN/XTAL_OUT buffers will remain enabled if REF_SEL = LOW.

The following table summarizes the operating states controlled by the $\overline{\text{RST}}$/DIV pin.

<table>
<tr><th>$\overline{\text{RST}}$/DIV</th><th>Operating Mode</th><th>Input Reference Divider</th></tr>
<tr><td>LOW</td><td>RESET</td><td>N/A</td></tr>
<tr><td>MID</td><td>Normal Operation</td><td>÷ 2</td></tr>
<tr><td>HIGH</td><td>Normal Operation</td><td>÷ 1</td></tr>
</table></td></tr>
</table>

168 CLGA Pin No.	Name	I/O	Type	Description
FEEDBACK BLOCK				
H1	FB_IN	IN	COLD SPARED LVCMOS or LVTTL	**Feedback input clock source.** This cold spared LVCMOS/LVTTL input can be driven directly from the FB_OUT pin or from a digital circuit which has the FB_OUT pin at its source.
J1	FB_OUT	OUT	LVCMOS	**Feedback output clock source.** This LVCMOS3.3 output is driven from the PLL. The FB_DS[3:0] and FB_PS[2:0] inputs determine the divider, inverter, enable/disable, and phase settings for this output. The FB_OUT pin should be used as the originating clock source for the FB_IN pin.
H3 J2 K2 L2	FB_DS3 FB_DS2 FB_DS1 FB_DS0	IN	3-LEVEL	**Feedback output division selector and controller.** These four ternary inputs are used to control the FB_OUT clock divider, inverter, and enable control. Table 1 lists the output behavior resulting from each combination of these pins.
K4 K3 J4	FB_PS2 FB_PS1 FB_PS0	IN	3-LEVEL	**Feedback output phase selector.** These three ternary inputs are used to control the FB_OUT phase alignment. Table 2 lists the output phase selections resulting from each combination of these pins.

168 CLGA Pin No.	Name	I/O	Type	Description
			CLOCK BANK 0	
N4	0Q0	OUT	LVCMOS	**Bank 0 clock output 0.** This LVCMOS output is driven from the PLL. The 0Q_DS[3:0] and 0Q_PS[1:0] inputs determine the divider, inverter, enable/disable, and phase settings for this output. This terminal is enabled as an LVCMOS output when the $\overline{CM}$/LV pin is LOW.
			LVDS	**Bank 0 positive LVDS output terminal.** This LVDS output is driven from the PLL. The 0Q_DS[3:0] and 0Q_PS[1:0] inputs determine the divider, inverter, enable/disable, and phase settings for this output. This terminal should drive the positive LVDS input terminal on the receiving device and is the complement of the 0Q1 LVDS output terminal. This terminal is enabled as an LVDS output when the $\overline{CM}$/LV pin is MID or HIGH.
N3	0Q1	OUT	LVCMOS	**Bank 0 clock output 1.** This LVCMOS output is driven from the PLL. The 0Q_DS[3:0] and 0Q_PS[1:0] inputs determine the divider, inverter, enable/disable, and phase settings for this output. This terminal is enabled as an LVCMOS output when the $\overline{CM}$/LV pin is LOW.
			LVDS	**Bank 0 negative LVDS output terminal.** This LVDS output is driven from the PLL. The 0Q_DS[3:0] and 0Q_PS[1:0] inputs determine the divider, inverter, enable/disable, and phase settings for this output. This terminal should drive the negative LVDS input terminal on the receiving device and is the complement of the 0Q0 LVDS output terminal. This terminal is enabled as an LVDS output when the $\overline{CM}$/LV pin is MID or HIGH.
M6 M5 L5 M4	0Q_DS3 0Q_DS2 0Q_DS1 0Q_DS0	IN	3-LEVEL	**0Q bank output division selector and controller.** These four ternary inputs are used to control the 0Q[1:0] output clock divider, inverter, and enable control. Table 1 lists the output behavior resulting from each combination of these pins.
M2 L3	0Q_PS1 0Q_PS0	IN	3-LEVEL	**0Q bank output phase selector.** These two ternary inputs are used to control the 0Q[1:0] output phase alignment. Table 2 lists the output phase selections resulting from each combination of these pins.
N5	V_{DD_0Q}	PWR	POWER	**0Q bank power supply.** +2.5V +/-10% or +3.3V +/-0.3V power source.
N2	V_{SS_0Q}	PWR	POWER	**0Q bank ground reference supply.** 0.0V ground reference source.

168 CLGA Pin No.	Name	I/O	Type	Description
CLOCK BANK 1				
N8	1Q0	OUT	LVCMOS	**Bank 1 clock output 0.** This LVCMOS output is driven from the PLL. The 1Q_DS[3:0] and 1Q_PS[1:0] inputs determine the divider, inverter, enable/disable, and phase settings for this output. This terminal is enabled as an LVCMOS output when the $\overline{\text{CM}}$/LV pin is LOW or MID.
			LVDS	**Bank 1 positive LVDS output terminal.** This LVDS output is driven from the PLL. The 1Q_DS[3:0] and 1Q_PS[1:0] inputs determine the divider, inverter, enable/disable, and phase settings for this output. This terminal should drive the positive LVDS input terminal on the receiving device and is the complement of the 1Q1 LVDS output terminal. This terminal is enabled as an LVDS output when the $\overline{\text{CM}}$/LV pin is HIGH.
N7	1Q1	OUT	LVCMOS	**Bank 1 clock output 1.** This LVCMOS output is driven from the PLL. The 1Q_DS[3:0] and 1Q_PS[1:0] inputs determine the divider, inverter, enable/disable, and phase settings for this output. This terminal is enabled as an LVCMOS output when the $\overline{\text{CM}}$/LV pin is LOW or MID.
			LVDS	**Bank 1 negative LVDS output terminal.** This LVDS output is driven from the PLL. The 1Q_DS[3:0] and 1Q_PS[1:0] inputs determine the divider, inverter, enable/disable, and phase settings for this output. This terminal should drive the negative LVDS input terminal on the receiving device and is the complement of the 1Q0 LVDS output terminal. This terminal is enabled as an LVDS output when the $\overline{\text{CM}}$/LV pin is HIGH.
K6 L7 K8 L8	1Q_DS3 1Q_DS2 1Q_DS1 1Q_DS0	IN	3-LEVEL	**1Q bank output division selector and controller.** These four ternary inputs are used to control the 1Q[1:0] output clock divider, inverter, and enable control. Table 1 lists the output behavior resulting from each combination of these pins.
L6 K5	1Q_PS1 1Q_PS0	IN	3-LEVEL	**1Q bank output phase selector.** These two ternary inputs are used to control the 1Q[1:0] output phase alignment. Table 2 lists the output phase selections resulting from each combination of these pins.
N9	V_{DD_1Q}	PWR	POWER	**1Q bank power supply.** +2.5V +/-10% or +3.3V +/-0.3V power source.
N6	V_{SS_1Q}	PWR	POWER	**1Q bank ground reference supply.** 0.0V ground reference source.

168 CLGA Pin No.	Name	I/O	Type	Description
				CLOCK BANK 2
N12	2Q0	OUT	LVCMOS	**Bank 2 clock output 0.** This LVCMOS output is driven from the PLL. The 2Q_DS[3:0] and 2Q_PS[1:0] inputs determine the divider, inverter, enable/disable, and phase settings for this output. This terminal is enabled as an LVCMOS output when the $\overline{CM}$/LV pin is LOW.
			LVDS	**Bank 2 positive LVDS output terminal.** This LVDS output is driven from the PLL. The 2Q_DS[3:0] and 2Q_PS[1:0] inputs determine the divider, inverter, enable/disable, and phase settings for this output. This terminal should drive the positive LVDS input terminal on the receiving device and is the complement of the 2Q1 LVDS output terminal. This terminal is enabled as an LVDS output when the $\overline{CM}$/LV pin is MID or HIGH.
N11	2Q1	OUT	LVCMOS	**Bank 2 clock output 1.** This LVCMOS output is driven from the PLL. The 2Q_DS[3:0] and 2Q_PS[1:0] inputs determine the divider, inverter, enable/disable, and phase settings for this output. This terminal is enabled as an LVCMOS output when the $\overline{CM}$/LV pin is LOW.
			LVDS	**Bank 2 negative LVDS output terminal.** This LVDS output is driven from the PLL. The 2Q_DS[3:0] and 2Q_PS[1:0] inputs determine the divider, inverter, enable/disable, and phase settings for this output. This terminal should drive the negative LVDS input terminal on the receiving device and is the complement of the 2Q0 LVDS output terminal. This terminal is enabled as an LVDS output when the $\overline{CM}$/LV pin is MID or HIGH.
K10 L10 L11 M10	2Q_DS3 2Q_DS2 2Q_DS1 2Q_DS0	IN	3-LEVEL	**2Q bank output division selector and controller.** These four ternary inputs are used to control the 2Q[1:0] output clock divider, inverter, and enable control. Table 1 lists the output behavior resulting from each combination of these pins.
M9 L9	2Q_PS1 2Q_PS0	IN	3-LEVEL	**2Q bank output phase selector.** These two ternary inputs are used to control the 2Q[1:0] output phase alignment. Table 2 lists the output phase selections resulting from each combination of these pins.
N10	V_{DD_2Q}	PWR	POWER	**2Q bank power supply.** +2.5V +/-10% or +3.3V +/-0.3V power source.
N13	V_{SS_2Q}	PWR	POWER	**2Q bank ground reference supply.** 0.0V ground reference source.

168 CLGA Pin No.	Name	I/O	Type	Description
CLOCK BANK 3				
J13	3Q0	OUT	LVCMOS	**Bank 3 clock output 0.** This LVCMOS output is driven from the PLL. The 3Q_DS[3:0] and 3Q_PS[1:0] inputs determine the divider, inverter, enable/disable, and phase settings for this output. This terminal is enabled as an LVCMOS output when the $\overline{\text{CM}}$/LV pin is LOW or MID.
			LVDS	**Bank 3 positive LVDS output terminal.** This LVDS output is driven from the PLL. The 3Q_DS[3:0] and 3Q_PS[1:0] inputs determine the divider, inverter, enable/disable, and phase settings for this output. This terminal should drive the positive LVDS input terminal on the receiving device and is the complement of the 3Q1 LVDS output terminal. This terminal is enabled as an LVDS output when the $\overline{\text{CM}}$/LV pin is HIGH.
K13	3Q1	OUT	LVCMOS	**Bank 3 clock output 1.** This LVCMOS output is driven from the PLL. The 3Q_DS[3:0] and 3Q_PS[1:0] inputs determine the divider, inverter, enable/disable, and phase settings for this output. This terminal is enabled as an LVCMOS output when the $\overline{\text{CM}}$/LV pin is LOW or MID.
			LVDS	**Bank 3 negative LVDS output terminal.** This LVDS output is driven from the PLL. The 3Q_DS[3:0] and 3Q_PS[1:0] inputs determine the divider, inverter, enable/disable, and phase settings for this output. This terminal should drive the negative LVDS input terminal on the receiving device and is the complement of the 3Q0 LVDS output terminal. This terminal is enabled as an LVDS output when the $\overline{\text{CM}}$/LV pin is HIGH.
H11 F10 F11 G11	3Q_DS3 3Q_DS2 3Q_DS1 3Q_DS0	IN	3-LEVEL	**3Q bank output division selector and controller.** These four ternary inputs are used to control the 3Q[1:0] output clock divider, inverter, and enable control. Table 1 lists the output behavior resulting from each combination of these pins.
H12 J11	3Q_PS1 3Q_PS0	IN	3-LEVEL	**3Q bank output phase selector.** These two ternary inputs are used to control the 3Q[1:0] output phase alignment. Table 2 lists the output phase selections resulting from each combination of these pins.
H13	V_{DD_3Q}	PWR	POWER	**3Q bank power supply.** +2.5V +/-10% or +3.3V +/-0.3V power source.
L13	V_{SS_3Q}	PWR	POWER	**3Q bank ground reference supply.** 0.0V ground reference source.

168 CLGA Pin No.	Name	I/O	Type	Description
CLOCK BANK 4				
D13	4Q0	OUT	LVCMOS	**Bank 4 clock output 0.** This LVCMOS output is driven from the PLL. The 4Q_DS[3:0] and 4Q_PS[1:0] inputs determine the divider, inverter, enable/disable, and phase settings for this output. This terminal is enabled as an LVCMOS output when the $\overline{CM}$/LV pin is LOW.
			LVDS	**Bank 4 positive LVDS output terminal.** This LVDS output is driven from the PLL. The 4Q_DS[3:0] and 4Q_PS[1:0] inputs determine the divider, inverter, enable/disable, and phase settings for this output. This terminal should drive the positive LVDS input terminal on the receiving device and is the complement of the 4Q1 LVDS output terminal. This terminal is enabled as an LVDS output when the $\overline{CM}$/LV pin is MID or HIGH.
E13	4Q1	OUT	LVCMOS	**Bank 4 clock output 1.** This LVCMOS output is driven from the PLL. The 4Q_DS[3:0] and 4Q_PS[1:0] inputs determine the divider, inverter, enable/disable, and phase settings for this output. This terminal is enabled as an LVCMOS output when the $\overline{CM}$/LV pin is LOW.
			LVDS	**Bank 4 negative LVDS output terminal.** This LVDS output is driven from the PLL. The 4Q_DS[3:0] and 4Q_PS[1:0] inputs determine the divider, inverter, enable/disable, and phase settings for this output. This terminal should drive the negative LVDS input terminal on the receiving device and is the complement of the 4Q0 LVDS output terminal. This terminal is enabled as an LVDS output when the $\overline{CM}$/LV pin is MID or HIGH.
E11 C12 D11 F12	4Q_DS3 4Q_DS2 4Q_DS1 4Q_DS0	IN	3-LEVEL	**4Q bank output division selector and controller.** These four ternary inputs are used to control the 4Q[1:0] output clock divider, inverter, and enable control. Table 1 lists the output behavior resulting from each combination of these pins.
L12 J10	4Q_PS1 4Q_PS0	IN	3-LEVEL	**4Q bank output phase selector.** These two ternary inputs are used to control the 4Q[1:0] output phase alignment. Table 2 lists the output phase selections resulting from each combination of these pins.
F13	V_{DD_4Q}	PWR	POWER	**4Q bank power supply.** +2.5V +/-10% or +3.3V +/-0.3V power source.
C13	V_{SS_4Q}	PWR	POWER	**4Q bank ground reference supply.** 0.0V ground reference source.

168 CLGA Pin No.	Name	I/O	Type	Description
CLOCK BANK 5				
A11	5Q0	OUT	LVCMOS	**Bank 5 clock output 0.** This LVCMOS output is driven from the PLL. The 5Q_DS[3:0] and 5Q_PS[1:0] inputs determine the divider, inverter, enable/disable, and phase settings for this output. This terminal is enabled as an LVCMOS output when the $\overline{CM}$/LV pin is LOW or MID.
			LVDS	**Bank 5 positive LVDS output terminal.** This LVDS output is driven from the PLL. The 5Q_DS[3:0] and 5Q_PS[1:0] inputs determine the divider, inverter, enable/disable, and phase settings for this output. This terminal should drive the positive LVDS input terminal on the receiving device and is the complement of the 5Q1 LVDS output terminal. This terminal is enabled as an LVDS output when the $\overline{CM}$/LV pin is HIGH.
A12	5Q1	OUT	LVCMOS	**Bank 5 clock output 1.** This LVCMOS output is driven from the PLL. The 5Q_DS[3:0] and 5Q_PS[1:0] inputs determine the divider, inverter, enable/disable, and phase settings for this output. This terminal is enabled as an LVCMOS output when the $\overline{CM}$/LV pin is LOW or MID.
			LVDS	**Bank 5 negative LVDS output terminal.** This LVDS output is driven from the PLL. The 5Q_DS[3:0] and 5Q_PS[1:0] inputs determine the divider, inverter, enable/disable, and phase settings for this output. This terminal should drive the negative LVDS input terminal on the receiving device and is the complement of the 5Q0 LVDS output terminal. This terminal is enabled as an LVDS output when the $\overline{CM}$/LV pin is HIGH.
D8 C11 C9 B9	5Q_DS3 5Q_DS2 5Q_DS1 5Q_DS0	IN	3-LEVEL	**5Q bank output division selector and controller.** These four ternary inputs are used to control the 5Q[1:0] output clock divider, inverter, and enable control. Table 1 lists the output behavior resulting from each combination of these pins.
D10 C10	5Q_PS1 5Q_PS0	IN	3-LEVEL	**5Q bank output phase selector.** These two ternary inputs are used to control the 5Q[1:0] output phase alignment. Table 2 lists the output phase selections resulting from each combination of these pins.
A10	V_{DD_5Q}	PWR	POWER	**5Q bank power supply.** +2.5V +/-10% or +3.3V +/-0.3V power source.
A13	V_{SS_5Q}	PWR	POWER	**5Q bank ground reference supply.** 0.0V ground reference source.

168 CLGA Pin No.	Name	I/O	Type	Description
		CLOCK BANK 6		
A7	6Q0	OUT	LVCMOS	**Bank 6 clock output 0.** This LVCMOS output is driven from the PLL. The 6Q_DS[3:0] and 6Q_PS[1:0] inputs determine the divider, inverter, enable/disable, and phase settings for this output. This terminal is enabled as an LVCMOS output when the $\overline{CM}$/LV pin is LOW.
			LVDS	**Bank 6 positive LVDS output terminal.** This LVDS output is driven from the PLL. The 6Q_DS[3:0] and 6Q_PS[1:0] inputs determine the divider, inverter, enable/disable, and phase settings for this output. This terminal should drive the positive LVDS input terminal on the receiving device and is the complement of the 6Q1 LVDS output terminal. This terminal is enabled as an LVDS output when the $\overline{CM}$/LV pin is MID or HIGH.
A8	6Q1	OUT	LVCMOS	**Bank 6 clock output 1.** This LVCMOS output is driven from the PLL. The 6Q_DS[3:0] and 6Q_PS[1:0] inputs determine the divider, inverter, enable/disable, and phase settings for this output. This terminal is enabled as an LVCMOS output when the $\overline{CM}$/LV pin is LOW.
			LVDS	**Bank 6 negative LVDS output terminal.** This LVDS output is driven from the PLL. The 6Q_DS[3:0] and 6Q_PS[1:0] inputs determine the divider, inverter, enable/disable, and phase settings for this output. This terminal should drive the negative LVDS input terminal on the receiving device and is the complement of the 6Q0 LVDS output terminal. This terminal is enabled as an LVDS output when the $\overline{CM}$/LV pin is MID or HIGH.
B10 C7 B4 D6	6Q_DS3 6Q_DS2 6Q_DS1 6Q_DS0	IN	3-LEVEL	**6Q bank output division selector and controller.** These four ternary inputs are used to control the 6Q[1:0] output clock divider, inverter, and enable control. Table 1 lists the output behavior resulting from each combination of these pins.
C8 B8	6Q_PS1 6Q_PS0	IN	3-LEVEL	**6Q bank output phase selector.** These two ternary inputs are used to control the 6Q[1:0] output phase alignment. Table 2 lists the output phase selections resulting from each combination of these pins.
A9	V_{DD_6Q}	PWR	POWER	**6Q bank power supply.** +2.5V +/-10% or +3.3V +/-0.3V power source.
A6	V_{SS_6Q}	PWR	POWER	**6Q bank ground reference supply.** 0.0V ground reference source.

168 CLGA Pin No.	Name	I/O	Type	Description
CLOCK BANK 7				
A3	7Q0	OUT	LVCMOS	**Bank 7 clock output 0.** This LVCMOS output is driven from the PLL. The 7Q_DS[3:0] and 7Q_PS[1:0] inputs determine the divider, inverter, enable/disable, and phase settings for this output. This terminal is enabled as an LVCMOS output when the $\overline{\text{CM}}$/LV pin is LOW or MID.
			LVDS	**Bank 7 positive LVDS output terminal.** This LVDS output is driven from the PLL. The 7Q_DS[3:0] and 7Q_PS[1:0] inputs determine the divider, inverter, enable/disable, and phase settings for this output. This terminal should drive the positive LVDS input terminal on the receiving device and is the complement of the 7Q1 LVDS output terminal. This terminal is enabled as an LVDS output when the $\overline{\text{CM}}$/LV pin is HIGH.
A4	7Q1	OUT	LVCMOS	**Bank 7 clock output 1.** This LVCMOS output is driven from the PLL. The 7Q_DS[3:0] and 7Q_PS[1:0] inputs determine the divider, inverter, enable/disable, and phase settings for this output. This terminal is enabled as an LVCMOS output when the $\overline{\text{CM}}$/LV pin is LOW or MID.
			LVDS	**Bank 7 negative LVDS output terminal.** This LVDS output is driven from the PLL. The 7Q_DS[3:0] and 7Q_PS[1:0] inputs determine the divider, inverter, enable/disable, and phase settings for this output. This terminal should drive the negative LVDS input terminal on the receiving device and is the complement of the 7Q0 LVDS output terminal. This terminal is enabled as an LVDS output when the $\overline{\text{CM}}$/LV pin is HIGH.
C5 C3 D7 B5	7Q_DS3 7Q_DS2 7Q_DS1 7Q_DS0	IN	3-LEVEL	**7Q bank output division selector and controller.** These four ternary inputs are used to control the 7Q[1:0] output clock divider, inverter, and enable control. Table 1 lists the output behavior resulting from each combination of these pins.
B6 C6	7Q_PS1 7Q_PS0	IN	3-LEVEL	**7Q bank output phase selector.** These two ternary inputs are used to control the 7Q[1:0] output phase alignment. Table 2 lists the output phase selections resulting from each combination of these pins.
A5	V_{DD_7Q}	PWR	POWER	**7Q bank power supply.** +2.5V +/-10% or +3.3V +/-0.3V power source.
A2	V_{SS_7Q}	PWR	POWER	**7Q bank ground reference supply.** 0.0V ground reference source.

<table>
<tr><th>168 CLGA
Pin No.</th><th>Name</th><th>I/O</th><th>Type</th><th>Description</th></tr>
<tr><td colspan="5">MISCELLANEOUS I/O</td></tr>
<tr><td>B2</td><td>TEST</td><td>IN</td><td>3-LEVEL</td><td>Test controller input.
This ternary input is used to enable the various test modes available with this device. The following table lists the available test modes:
<table><tr><th>TEST*</th><th>Selected Source</th></tr><tr><td>L</td><td>Normal Operation</td></tr><tr><td>M</td><td>REF bypass PLL</td></tr><tr><td>H</td><td>FB_IN bypass PLL</td></tr></table>
Note* Whenever TEST does not equal the L state, the internal oscillator will be held in reset.</td></tr>
<tr><td>K11</td><td>FREQ_SEL</td><td>IN</td><td>3-LEVEL</td><td>PLL operating frequency range selection.
This ternary input selects the nominal operating frequency range in which the PLL oscillates.

The following table shows the PLL frequency range selected by this input.
<table><tr><th>FREQ_SEL</th><th>Nominal PLL
Frequency Range (f_{PLL})</th></tr><tr><td>L</td><td>24 MHz to 50 MHz</td></tr><tr><td>M</td><td>48 MHz to 100 MHz</td></tr><tr><td>H</td><td>96 MHz to 200 MHz</td></tr></table></td></tr>
<tr><td>D9</td><td>$\overline{\text{sOE}}$</td><td>IN</td><td>LVCMOS or LVTTL</td><td>Synchronous output enable.
This LVCMOS/LVTTL input synchronously enables/disables the nQ[1:0] pins. Each clock output that is controlled by the $\overline{\text{sOE}}$ pin is synchronously enabled/disabled by the individual output clock. When HIGH, sOE forces all clocks to a LOW level, unless individual clock banks have been disabled by the nQ_DS [3:0] settings.</td></tr>
</table>

168 CLGA Pin No.	Name	I/O	Type	Description
H10	$\overline{\text{CM}}$/LV	IN	3-LEVEL	**CMOS/LVDS clock bank signaling selector.** This ternary input controls whether nQ[1:0] outputs drive LVCMOS or LVDS signalling. The following table shows the output signalling that is selected by this input.

		$\overline{\text{CM}}$/LV		
		HIGH	**MID**	**LOW**
Banks	**0Q**	**LVDS**	**LVDS**	**LVCMOS**
	1Q	**LVDS**	**LVCMOS**	**LVCMOS**
	2Q	**LVDS**	**LVDS**	**LVCMOS**
	3Q	**LVDS**	**LVCMOS**	**LVCMOS**
	4Q	**LVDS**	**LVDS**	**LVCMOS**
	5Q	**LVDS**	**LVCMOS**	**LVCMOS**
	6Q	**LVDS**	**LVDS**	**LVCMOS**
	7Q	**LVDS**	**LVCMOS**	**LVCMOS**

<table>
<tr><th>168 CLGA
Pin No.</th><th>Name</th><th>I/O</th><th>Type</th><th>Description</th></tr>
<tr><td>D4</td><td>LOCK</td><td>OUT</td><td>LVCMOS</td><td>
PLL lock indication signal.
This LVCMOS output informs the system that the PLL is locked onto the reference and FB_IN clocks. A HIGH state indicates that the PLL is in a locked condition. A LOW state indicates that the PLL is not locked and the outputs may not be stable or synchronized to the reference clock source. As indicated in Table 10.0, AC Electrical Characteristics for LVCMOS Outputs, the level of phase alignment between the reference and FB_IN that will cause the LOCK pin to signal a "LOCKED" condition is dependent upon the frequency range selected by the FREQ_SEL input.
After the LOCK pin is asserted HIGH, indicating the reference clock and FB_IN are stable and phase aligned per the above table. The LOCK pin will de-assert to a LOW state when the Reference and FB_IN clock separate by more than the above amount. Special conditions apply when the device is placed in either test or reset mode. When in test mode, (TEST=MID or HIGH), all ternary inputs are NANDed to drive the LOCK output. When in reset mode (RST/DIV=LOW, TEST= LOW), the LOCK output is driven HIGH. These conditions are summarized in the following table.
<table>
<tr><th>$\overline{RST}$/DIV</th><th>TEST</th><th>LOCK</th></tr>
<tr><td>M/H</td><td>L</td><td>LOCK=HIGH if REF+FB_IN are aligned. LOCK=LOW otherwise</td></tr>
<tr><td>L</td><td>L</td><td>HIGH</td></tr>
<tr><td>Don’t Care</td><td>M/H</td><td>LOCK=HIGH if all ternary inputs are LOW. LOCK=LOW if any ternary input is not LOW</td></tr>
</table>
</td></tr>
</table>

168 CLGA Pin No.	Name	I/O	Type	Description
B1, B3, B7, B12, B13, D2, D3, D12, E5, E6, E9, E10, F4, F5, F9, G2, G4, G10, G12, H2, H5, H9, J3, J5, J6, J8, J9, K7, K12, M3, M7, M12, M13, N1	V_{DD_C}	PWR	POWER	**Core power supply.** +3.3V +/-0.3V power source. This power supply must be operated at the same potential as the analog power supply.
B11, C2, C4, D5, E4, E7, E8, E12, F1, F6, F7, F8, G3, G5, G6, G7, G8, G9, G13, H4, H6, H7, H8, J7, J12, K1, K9, L4, M8, M11	V_{SS_C}	PWR	POWER	**Core ground reference supply.** 0.0V ground reference source.
E1, E2	V_{DD_A}	PWR	POWER	**Analog power supply.** +3.3V +/-0.3V power source. This power supply must be operated at the same potential as the core power supply.
E3	V_{SS_A}	PWR	POWER	**Analog ground reference supply.** 0.0V ground reference source.

5.0 ABSOLUTE MAXIMUM RATINGS:[1]

(Referenced to $V_{SS\_A/C/nQ}$)

Symbol	Description	Limits	Units
V_{DD_C} & V_{DD_A}	Core Power Supply Voltage	-0.3 to 4.0	V
V_{DD_0Q} through V_{DD_7Q}	Output Bank Power Supply Voltage	-0.3 to 4.0	V
V_{IN_C}	Voltage Any Core Input Pin	-0.3 to V_{DD_C} + 0.3	V
V_{IN_R}	Voltage Any Reference Input Pin	-0.3 to V_{DD_C} + 0.3	V
V_{IN_FB}	Voltage FB_IN Input Pin	-0.3 to V_{DD_C} + 0.3	V
V_{OUT_LVCMOS}	Voltage Any Clock Bank Output	-0.3 to V_{DD_nQ} + 0.3	V
V_{OUT_LVDS}	Voltage Any Clock Bank Output	-0.3 to V_{DD_nQ} + 0.3	V
V_O	Voltage on XTAL_OUT, FB_OUT, and LOCK Outputs	-0.3 to V_{DD_C} + 0.3	V
I_I	DC Input Current	±10	mA
P_D [2]	Maximum Power Dissipation Permitted @ T_C = +125°C	5	W
T_{STG}	Storage Temperature	-65 to +150	°C
T_J [3]	Maximum Junction Temperature	+150	°C
$\Theta_{JC\text{-}168CLGA}$	Thermal Resistance, Junction to Case (168-CLGA)	5	°C/W
ESD_{HBM}	ESD Protection (Human Body Model) - Class I	750	V

Notes:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2. Per MIL-STD-883, Method 1012, Section 3.4.1, $\mathbf{P_D = (T_J(max) - T_C(max)) / \Theta_{JC}}$
3. Maximum junction temperature may be increased to +175°C during burn-in and steady-static life.

6.0 RECOMMENDED OPERATING CONDITIONS

Symbol	Description		Limits	Units
V_{DD_C} & V_{DD_A}	Core and Analog Power Supply Voltage		3.0 to 3.6	V
V_{DD_0Q} through V_{DD_7Q}	Output Bank Operating Voltage		2.25 to 3.6	V
$V_{IN\_CONTROL}$	Voltage Any Configuration and Control Input		0 to V_{DD_C}	V
V_{IN_REF}	Voltage REF Input		0 to V_{DD_C}	V
V_{IN_XTAL}	Voltage XTAL_IN Input		0 to V_{DD_C}	V
V_{IN_LVDIN}	Voltage LVDS Input		2.4	V
V_{IN_FB}	Voltage FB_IN Input		0 to V_{DD_C}	V
V_{OUT_LOCK}	Voltage LOCK Output		0 to V_{DD_C}	V
V_{OUT_XTAL}	Voltage XTAL_OUT Output		0 to V_{DD_C}	V
V_{OUT_nQ}	Voltage Any LVCMOS Clock Bank Output		0 to V_{DD_nQ}	V
V_{OUT_LVDS}	Voltage LVDS Outputs		0.925 to 1.65	V
V_{OUT_FB}	Voltage FB_OUT Output		0 to V_{DD_C}	V
T_C	Case Operating Temperature	HiRel	-55 to +125	°C

Notes:

1. When configuring an output bank for LVDS drive, the corresponding V_{DD_NQ} range is 3.0 to 3.6V.

7.0 DC ELECTRICAL CHARACTERISTICS 3-LEVEL and LVCMOS/LVTTL INPUTS

($V_{DD\_A/C}$ = +3.3V ± 0.3V; T_C is per the screening level ordered)*

Symbol	Description	Conditions	Min.	Max.	Units
V_{IH}	High-level input voltage (REF, FB_IN, and $\overline{sOE}$)		+2.0	--	V
V_{IL}	Low-level input voltage (REF, FB_IN, and $\overline{sOE}$)		--	+0.8	V
V_{IHH} [1]	High-level input voltage	Ternary Inputs	V_{DD_C} - 0.6	--	V
V_{IMM} [1]	Mid-level input voltage	Ternary Inputs	(V_{DD_C}/2) - 0.3	(V_{DD_C}/2) + 0.3	V
V_{ILL} [1]	Low-level input voltage	Ternary Inputs	--	+0.6	V
V_{IC+}	Positive input clamp voltage (except REF and FB_IN pin)	For input under test: I_{IN} = +18mA; $V_{DD\_A/C}$ = 0.0V	+0.4	+1.5	V
V_{IC-}	Negative input clamp voltage (all inputs)	For input under test: I_{IN} = -18mA; $V_{DD\_A/C}$ = 0.0V	-1.5	-0.4	V
I_{CS}	Input cold spare leakage (REF, FB_IN)	For input under test: V_{IN} = +3.6V; V_{DD_C} = 0.0V ±0.3V	-5	+5	µA
I_{IL-2L}	Input leakage current on 2-level inputs	For input under test: V_{IN} = +3.6V or 0.0V; $V_{DD\_A/C}$ = +3.6V; Pin: $\overline{sOE}$	-1	+1	µA
		Pins: REF, FB_IN	-5	5	µA
I_{3L} [1]	3-level input DC current	HIGH, V_{IN} = V_{DD_C}	--	+200	µA
		MID, V_{IN} = V_{DD_C}/2	-50	+50	µA
		LOW, V_{IN} = V_{SS_C}	-200	--	µA
C_{IN-2L} [2]	Input pin capacitance (2-level inputs)	*f* = 1MHz @ 0V; REF, FB_IN	6 (typical)		pF
		f = 1MHz @ 0V; $\overline{sOE}$	9 (typical)		pF
C_{IN-3L} [2]	Input pin capacitance (3-level inputs)	*f* = 1MHz @ 0V	12 (typical)		pF

Notes:

* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1. These inputs are normally wired to V_{DD_C}, V_{SS_C}, or left unconnected. Internal termination resistors bias unconnected inputs to V_{DD_C}/2 ± 0.3V.
2. Capacitance is measured for initial qualification and when design changes may affect the input/output capacitance. Capacitance is measured between the designated terminal and V_{SS_C} at a frequency of 1MHz and a signal amplitude of 50mV rms maximum.

7.1 DC ELECTRICAL CHARACTERISTICS LVDS INPUTS[1]

($V_{DD\_A/C}$ = +3.3V ± 0.3V; T_C is per the screening level ordered)*

Symbol	Description	Conditions	Min.	Max.	Units
I_{LVDIN}	Input leakage current	For input under test V_{IN} = +3.6V or 0.0V; V_{DD_C} = +3.6V	-15	+15	µA
V_{TH} [2]	Differential input high threshold	V_{CM} = +1.2V	V_{CM}+0.1		V
V_{TL} [2]	Differential input low threshold	V_{CM} = +1.2V		V_{CM}-0.1	V
V_{CMR} [4]	Common mode voltage range	V_{ID} = 200mV peak-to-peak	0.1	2.3	V
I_{CS}	Input cold spare leakage	For input under test V_{IN} = +3.6V; V_{DD_C} = 0.0V	-5	+5	µA
V_{IC-}	Negative input clamp voltage	For Input Under Test: I_{IN} = -18mA	-1.5	-0.4	V
C_{LVDIN} [3]	Input pin capacitance	*f* = 1MHz @ 0V	7		pF

Notes:
* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.
1. LVDS compatible input pins include: LVDIN+, LVDIN-.
2. Guaranteed by characterization, and functionally tested.
3. Capacitance is measured for initial qualification and when design changes may affect the input/output capacitance. Capacitance is measured between the designated terminal and V_{SS_C} at a frequency of 1MHz and a signal amplitude of 50mV rms maximum.
4. Guaranteed by characterization, but not tested.

7.2 DC ELECTRICAL CHARACTERISTICS XTAL_IN INPUT

($V_{DD\_A/C}$ = +3.3V ± 0.3V; T_C is per the screening level ordered)*

Symbol	Description	Conditions	Min.	Max.	Units
V_{IH}	High-level input voltage		0.55 * V_{DD_C}	--	V
V_{IL}	Low-level input voltage		--	0.35 * V_{DD_C}	V
I_{XTAL_IN}	Input leakage current	For input under test V_{IN} = +3.6V or 0.0V; V_{DD_C} = +3.6V	-1	+1	µA
V_{IC+}	Positive input clamp voltage	For input under test: I_{IN} = +18mA; V_{DD_C} = 0.0V	+0.4	+1.5	V
V_{IC-}	Negative input clamp voltage	For Input Under test: I_{IN} = -18mA	-1.5	-0.4	V
C_{XTAL_IN} [1]	Input pin capacitance	*f* = 1MHz @ 0V	10		pF

Notes:
* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.
1. Capacitance is measured for initial qualification and when design changes may affect the input/output capacitance. Capacitance is measured between the designated terminal and V_{SS_C} at a frequency of 1MHz and a signal amplitude of 50mV rms maximum.

8.0 DC ELECTRICAL CHARACTERISTICS LVCMOS3.3 OUTPUTS[1]

(V_{DD_nQ} = +3.3V $\pm$ 0.3V; $V_{DD\_A/C}$ = +3.3V $\pm$ 0.3V; T_C is per the screening level ordered)*

Symbol	Description	Conditions		Min.	Max.	Units
V_{OL}	Low-level output voltage	I_{OL} = 12mA (Pins: nQ[1:0]; FB_OUT)	T_C = Room, Cold	--	0.4	V
			T_C = Hot	--	0.6	V
		I_{OL} = 2mA (Pin: LOCK)		--	0.4	V
V_{OH}	High-level output voltage	I_{OH} = -12mA (Pins: nQ[1:0]; FB_OUT)		2.4	--	V
		I_{OH} = -2mA (Pin: LOCK)		2.4	--	V
I_{OZ}	Output three-state current	nQ1 or nQ0 = 0V or V_{DD_nQ}, V_{DD_nQ} = +3.6V		-10	+10	μA
C_{OUT} [2]	Output pin capacitance	*f* = 1MHz @ 0V		13	13	pF

Notes:
* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.
1. LVCMOS3.3 compatible output pins include: FB_OUT, LOCK, 0Q[1:0], 1Q[1:0], 2Q[1:0], 3Q[1:0], 4Q[1:0], 5Q[1:0], 6Q[1:0], 7Q[1:0].
2. Capacitance is measured for initial qualification and when design changes may affect the input/output capacitance. Capacitance is measured between the designated terminal and V_{SS_nQ} at a frequency of 1MHz and a signal amplitude of 50mV rms maximum.

8.1 DC ELECTRICAL CHARACTERISTICS LVCMOS2.5 OUTPUTS[1]

(V_{DD_nQ} = +2.5V $\pm$ 10%; $V_{DD\_A/C}$ = +3.3V $\pm$ 0.3V; T_C is per the screening level ordered)*

Symbol	Description	Conditions		Min.	Max.	Units
V_{OL}	Low-level output voltage Pins: nQ[1:0]	I_{OL} = 6mA; V_{DD_nQ} = +2.25V; $V_{DD\_A/C}$=3.3V		--	0.4	V
		I_{OL} = 8mA; V_{DD_nQ} = +2.375V; $V_{DD\_A/C}$=3.3V		--	0.4	V
V_{OH}	High-level output voltage Pins: nQ[1:0]	I_{OH} = -6mA; V_{DD_nQ} = +2.25V; $V_{DD\_A/C}$=3.3V	T_C = Room, Cold	2.0	--	V
			T_C = Hot	1.9	--	V
		I_{OH} = -8mA; V_{DD_nQ} = +2.375V; $V_{DD\_A/C}$=3.3V	T_C = Room, Cold	2.0	--	V
			T_C = Hot	1.9	--	V
C_{OUT} [2]	Output pin capacitance	*f* = 1MHz @ 0V		13	13	pF

Notes:
* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.
1. LVCMOS2.5 compatible output pins include: 0Q[1:0], 1Q[1:0], 2Q[1:0], 3Q[1:0], 4Q[1:0], 5Q[1:0], 6Q[1:0], 7Q[1:0].
2. Capacitance is measured for initial qualification and when design changes may affect the input/output capacitance. Capacitance is measured between the designated terminal and V_{SS_nQ} at a frequency of 1MHz and a signal amplitude of 50mV rms maximum.

8.2 DC ELECTRICAL CHARACTERISTICS LVDS OUTPUTS[1,2]

(V_{DD_nQ} = +3.3V ± 0.3V; $V_{DD\_A/C}$ = +3.3V ± 0.3V; T_C is per the screening level ordered)*

Symbol	Description	Conditions	Min.	Max.	Units
V_{OL}	Low-level output voltage	R_L = 100Ω (see figure 9)	0.925		V
V_{OH}	High-level output voltage	R_L = 100Ω (see figure 9)		1.650	V
V_{OD}[2]	Differential output voltage	R_L = 100Ω (see figure 9)	250	400	mV
ΔV_{OD}[2]	Change in magnitude of V_{OD} for complementary output states	R_L = 100Ω (see figure 9)		35	mV
V_{OS}	Offset voltage	R_L = 100Ω , $\left(Vos = \frac{Voh + Vol}{2}\right)$ (see figure 9)	1.125	1.450	V
ΔV_{OS}	Change in magnitude of V_{OS} for complementary output states	R_L = 100Ω (see figure 9)		25	mV
I_{OS}	Output short circuit current	nQ1 or nQ0 = V_{SS_nQ} or V_{DD_nQ} V_{DD_nQ} = +3.6V	-10	10	mA
I_{OZ}	Output three-state current	nQ1 or nQ0 = V_{SS_nQ} or V_{DD_nQ}, V_{DD_nQ} = +3.6V	-10	+10	µA
C_{OUT}[3]	Output pin capacitance	*f* = 1MHz @ 0V	13		pF

Notes:
* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.
1. LVDS compatible output pins include: 0Q[1:0], 1Q[1:0], 2Q[1:0], 3Q[1:0], 4Q[1:0], 5Q[1:0], 6Q[1:0], 7Q[1:0].
2. All voltages are referenced to V_{SS} except for differential voltages.
3. Capacitance is measured for initial qualification and when design changes may affect the input/output capacitance. Capacitance is measured between the designated terminal and V_{SS_nQ} at a frequency of 1MHz and a signal amplitude of 50mV rms maximum.

8.3 DC ELECTRICAL CHARACTERISTICS XTAL_OUT OUTPUT

($V_{DD\_A/C}$ = +3.3V ± 0.3V; T_C is per the screening level ordered)*

Symbol	Description	Conditions		Min.	Max.	Units
V_{OL}	Low-level output voltage	I_{OL} = 16mA	T_C = Room, Cold	--	0.4	V
			T_C = Hot	--	0.5	
V_{OH}	High-level output voltage	I_{OH} = -16mA		2.4	--	V
C_{OUT}[1]	Output pin capacitance	*f* = 1MHz @ 0V		15		pF

Notes:
* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.
1. Capacitance is measured for initial qualification and when design changes may affect the input/output capacitance. Capacitance is measured between the designated terminal and V_{SS_C} at a frequency of 1MHz and a signal amplitude of 50mV rms maximum.

9.0 AC INPUT ELECTRICAL CHARACTERISTICS

($V_{DD\_A/C}$ = +3.3V $\pm$ 0.3V; T_C is per the screening level ordered)*

Symbol	Description	Condition		Min.	Max.	Unit
t_R, t_F [2]	Input rise/fall time	VIH(min)-VIL(max)	Pins: REF, FB_IN	--	20	ns
		VTH(min)-VTL(max)	Pins: LVDIN+, LVDIN-	--	20	
t_{PWC} [3,4]	Input clock pulse width	HIGH or LOW; REF		2	--	ns
t_{PER} [3,5,6,7]	Input clock period	$1 \div f_{REF}$		5	500	ns
f_{REFDET} [8]	Ref clock detector frequency	FREQ_SEL = LOW; $\overline{RST}$/DIV = HIGH;		--	100	KHz
f_{REF} [3,5,6]	Reference clock frequency	FREQ_SEL = LOW; $\overline{RST}$/DIV = HIGH		2.0	50	MHz
		FREQ_SEL = LOW; $\overline{RST}$/DIV = MID		4.0	100	MHz
		FREQ_SEL = MID; $\overline{RST}$/DIV = HIGH		2.0	100	MHz
		FREQ_SEL = MID; $\overline{RST}$/DIV = MID		4.0	200	MHz
		FREQ_SEL = HIGH; $\overline{RST}$/DIV = HIGH		3	200	MHz
		FREQ_SEL = HIGH; $\overline{RST}$/DIV = MID		6	200	MHz
t_{RESET}	Reset duration	Reference clock and all control inputs are stable and valid while RST/DIV is low		400	--	ns

Notes:

* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1. Reference Figure 8 for clock output loading circuit that is equivalent to the load circuit used for all AC testing. The input waveform used to test these parameters is shown in Figure 7.
2. Characterized in lab through functional testing.
3. Guaranteed by functional testing except where characterized.
4. For REF_SEL = HIGH, this parameter is guaranteed by characterization, but not tested. For REF_SEL=LOW, this parameter is not applicable.
5. Although the input reference frequencies are defined as-low-as 2MHz, the N and R dividers must be selected to ensure the PLL operates from 24MHz-50MHz when FREQ_SEL = LOW, 48MHz-100MHz when FREQ_SEL = MID, and 96MHz-200MHz when FREQ_SEL = HIGH.
6. XTAL_IN is characterized for crystal operation over V_{DD_C} and temperature corners using 2MHz, 24MHz, 48MHz, and 66.667MHz crystals which were configured in accordance with figure 3.
7. For REF_SEL = LOW, this parameter is guaranteed by laboratory characterization through functional testing of the XTAL_IN pin with a digital input clock signal at 2MHz and 62.5MHz in accordance with the test waveform in figure 7C.
8. Maximum REF frequency in which the UT7R2XLR816 will ignore the REF input and place the PLL into a pre-charge oscillator state.

10.0 AC ELECTRICAL CHARACTERISTICS FOR LVCMOS OUTPUTS

(V_{DD_nQ} = +2.5V $\pm$10% or +3.3V $\pm$ 0.3V; $V_{DD\_A/C}$ = +3.3V $\pm$ 0.3V; T_C is per the screening level ordered)*

Symbol	Description	Condition		Min.	Max.	Unit
f_{OR} [6]	Output frequency range			0.75	200	MHz
VCO_{LR} [6]	VCO lock range			24	200	MHz
t_{PD0} [2, 5]	Reference to FB_IN propagation delay	V_{DD_C} = +3.3V; T_C = Room Temperature		-150	+150	ps
t_{n*tu} [7]	Accuracy of phase selection time units	Skew accuracy from any output bank to any output bank configured to a valid number of skew steps, without division or inversion.		($n*t_U$-300)	($n*t_U$+300)	ps
t_{PART} [5]	Part-part skew	Skew between the outputs of any two devices under identical settings and conditions (V_{DD_nQ}, $V_{DD\_A/C}$, temp, air flow, frequency, etc).		--	250	ps
$t_{ODCV\text{-}LVCMOS}$ [5]	Output duty cycle LVCMOS Outputs	fout $\leq$ 100 MHz, measured at (V_{DD_nQ})/2	Figure 8B	45	55	%
			Figure 8C (Note 5)	45	55	
			Figure 8A (Note 5)	45	55	
		fout > 100 MHz, measured at (V_{DD_nQ})/2	Figure 8B	40	60	%
			Figure 8C (Note 5)	40	60	
			Figure 8A (Note 5)	40	60	
t_{PWH} [5]	Output high time pulse width	Measured at 0.5* V_{DD_nQ} + 0.5V f_{REF}=200MHz	V_{DD_nQ}= 3.3V Outputs loaded per Fig. 8A	1.5	--	ns
			V_{DD_nQ}= 2.5V Outputs loaded per Fig. 8A	1.5	--	
			V_{DD_nQ}= 3.3V Outputs loaded per Fig. 8B	1.5	--	
			V_{DD_nQ}= 2.5V Outputs loaded per Fig. 8B	1.5	--	
t_{PWL} [5]	Output low time pulse width	Measured at 0.5* V_{DD_nQ} - 0.5V f_{REF}=200MHz	V_{DD_nQ}= 3.3V Outputs loaded per Fig. 8A	2	--	ns
			V_{DD_nQ}= 2.5V Outputs loaded per Fig. 8A	2	--	
			V_{DD_nQ}= 3.3V Outputs loaded per Fig. 8B	2	--	
			V_{DD_nQ}= 2.5V Outputs loaded per Fig. 8B	2	--	
t_{LOCK} [3]	PLL lock time	$\overline{RST}$/DIV = MID or HIGH to LOCK = STABLE HIGH		--	1.0	ms
$t_{LOCKRES}$ [4,5]	LOCK Pin Resolution Maximum phase difference between reference and FB_IN to maintain LOCK	FREQ_SEL = LOW and MID			0.9	ns
		FREQ_SEL = HIGH			0.5	ns

Symbol	Description	Condition		Min.	Max.	Unit
$t_{ORISE-LVCMOS}$[5]	LVCMOS output rise time Figure 8A	Measured as transition time from $V_{OL(max)}$ to $V_{OH(min)}$ for $V_{DD\_A/C}$ = 3.3V; V_{DD_nQ} = 2.25V; $\overline{CM}$/LV= LOW f_{REF}=1MHz	FREQ_SEL=LOW or MID		3.0	ns
			FREQ_SEL=HIGH		2.75	ns
		Measured as transition time from $V_{OL(max)}$ to $V_{OH(min)}$ for $V_{DD\_A/C}$ = 3.3V; V_{DD_nQ} = 3.6V; $\overline{CM}$/LV= LOW f_{REF}=1MHz	FREQ_SEL=LOW or MID		1.25	ns
			FREQ_SEL=HIGH		1.0	ns
$t_{OFALL-LVCMOS}$[5]	LVCMOS output fall time Figure 8A	Measured as transition time from $V_{OH(min)}$ to $V_{OL(max)}$ for $V_{DD\_A/C}$ = 3.3V; V_{DD_nQ} = 2.25V; $\overline{CM}$/LV= LOW f_{REF}=1MHz	FREQ_SEL=LOW or MID		2.25	ns
			FREQ_SEL=HIGH		2.0	ns
		Measured as transition time from $V_{OH(min)}$ to $V_{OL(max)}$ for $V_{DD\_A/C}$ = 3.3V; V_{DD_nQ} = 3.6V; $\overline{CM}$/LV= LOW f_{REF}=1MHz	FREQ_SEL=LOW or MID		2.0	ns
			FREQ_SEL=HIGH		1.75	ns

Notes:

* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1. All outputs are equally loaded. See figure 8B.
2. t_{PD0} is measured at 1.5V for V_{DD_C} = +3.3V with REF rise/fall times of 1ns between 0.8V-2.0V.
3. t_{LOCK} is the time that is required before outputs synchronize to the reference input as determined by the phase alignment between the selected reference and FB_IN. This specification is valid with stable input reference clock and power supplies that are within normal operating limits.
4. The lock detector circuit will monitor the phase alignment between the selected reference input and FB_IN. When the phase separation between these two inputs is greater than the amount listed, the LOCK pin will drop low signaling that the PLL is out of lock.
5. Guaranteed by characterization, but not tested.
6. Guaranteed by functional testing.
7. The time unit t_U is calculated by equation 1 using the PLL operating frequency (see Table 3) and the multiplication factor determined by the state of the FREQ_SEL pin (see Table 5). Valid phase selection steps for each output clock bank are identified in Table 2.

10.1 AC ELECTRICAL CHARACTERISTICS FOR LVDS OUTPUTS

(V_{DD_nQ} = +3.3V $\pm$ 0.3V; $V_{DD\_A/C}$ = +3.3V $\pm$ 0.3V; T_C is per screening level ordered)*

Symbol	Description	Condition	Min.	Max.	Unit
t_{n*tu} [3,4]	Accuracy of phase selection time units	Skew accuracy from FB_OUT to any output bank configured to a valid number of skew step, without division or inversion.	($n*t_U$-300)	($n*t_U$+300)	ps
t_{PART} [2]	Part-part skew	Skew between the outputs of any two devices under identical settings and conditions (V_{DD_nQ}, $V_{DD\_A/C}$, temp, air flow, frequency, etc)	--	250	ps
$t_{ODCV\text{-}LVDS}$ [2]	Output duty cycle LVDS Outputs	fout $\leq$ 100 MHz, measured at VOS (Figure 10)	48	52	%
		fout > 100 MHz, measured at VOS (Figure 10)	45	55	%
$t_{ORISE\text{-}LVDS}$ [2]	LVDS output rise time	Measured as transition time between 20% V_{DIFF} and 80% V_{DIFF} (Figure 10) $\overline{CM}$/LV=HIGH; f_{REF}=1MHz		1.25	ns
$t_{OFALL\text{-}LVDS}$ [2]	LVDS output fall time	Measured as transition time between 80% V_{DIFF} and 20% V_{DIFF} (Figure 10) $\overline{CM}$/LV=HIGH; f_{REF}=1MHz		1.25	ns

Notes:
* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.
1. All outputs are equally loaded. See figure 9.
2. Guaranteed by characterization, but not tested.
3. The time unit t_U is calculated by equation 1 using the PLL operating frequency (see Table 3) and the multiplication factor determined by the state of the FREQ_SEL pin (see Table 5). Valid phase selection steps for each output clock bank are identified in Table 2.
4. Guaranteed by characterization and testing with LVCMOS buffers.

11.0 RECOMMENDED QUARTZ CRYSTAL SPECIFICATIONS

(Parallel Resonant Mode; Fundamental and Third Overtone)

Description	Conditions	Min.	Max.	Units
Frequency range	Fundamental	2.0		MHz
	Third Overtone		50	
Frequency tolerance		User Defined		ppm
Frequency to temperature stability		-100	+100	ppm
Aging		-5	+5	ppm/ year
Load capacitance	Parallel load	10	30	pF
Shunt capacitance	Frequency dependant	--	7	pF
Equivalent series resistance (ESR)	Frequency dependant	25	3000	Ω
Drive level		--	1.0	mW

12.0 POWER DISSIPATION CHARACTERISTICS

(Unless otherwise noted, V_{DD_nQ} = +2.5V ±10% or +3.3V ± 0.3V; $V_{DD\_A/C}$ = +3.3V ± 0.3V; T_C is per the screening level ordered)*

Symbol	Description	Conditions		Min.	Max.	Units
I_{DDRSTC}	RESET Core Power Supply Current	$V_{DD\_A/C}$ = +3.6V; sOE = HIGH; FB_IN = FB_OUT; REF, LVDIN+, LVDIN-, XTAL_IN, RST/DIV, FREQ_SEL, & TEST = LOW; All other inputs are floated; Outputs are not loaded	T_C = Room, Cold	--	+1.40	mA
			T_C = Hot	--	+1.40	mA
SI_{DD_C}	Standby Core Power Supply Current	$V_{DD\_A/C}$ = +3.6V; sOE, RST/DIV, FREQ_SEL = HIGH; FB_IN = FB_OUT; REF, LVDIN+, LVDIN-, XTAL_IN, CM/LV, and TEST = LOW; All other inputs are floated; Outputs are not loaded		--	+170	mA
AI_{DD_C}	Active core power supply current	$V_{DD\_A/C}$ = +3.6V; RST/DIV = HIGH; FB_IN = FB_OUT; sOE, LVDIN+, LVDIN-, XTAL_IN, FREQ_SEL, and TEST = LOW; All other inputs are floated; Outputs are not loaded	REF = 2MHz PLL = 24MHz	--	+40	mA
			REF = 200MHz PLL = 200MHz	--	290	
AI_{DD_nQ33} (Notes 1,2)	Dynamic output bank supply current	LVCMOS3.3 Outputs REF = 2MHz and 200MHz; sOE = LOW; V_{DD_nQ} = +3.6V; C_L = 40pF/output;	nQ[1:0] = 24MHz	--	12	mA/ Bank
			nQ[1:0] = 200MHz	--	23	
AI_{DD_nQ25} (Notes 1,2)	Dynamic output bank supply current	LVCMOS2.5 Outputs REF = 2MHz and 200MHz; sOE = LOW; V_{DD_nQ} = +2.75V; C_L = 40pF/output;	nQ[1:0] = 24MHz	--	8.75	mA/ Bank
			nQ[1:0] = 200MHz	--	17	
AI_{DD_CLVDS} (Notes 2,3)	Core power supply current when LVDS output banks are running	$V_{DD\_A/C}$ = V_{DD_nQ} = +3.6V; RST/DIV = CM/LV = HIGH; FB_IN = FB_OUT; sOE, FREQ_SEL, and TEST = LOW; All other ternary inputs are floated; C_L = 40pF/output; R_L = 100Ω Differential	REF = 2MHz PLL = 24MHz nQ[1:0] = 24MHz	--	75	mA
			REF = 200MHz PLL = 200MHz nQ[1:0] = 200MHz	--	340	
AI_{DD_nQLVDS} (Notes 2,3)	Dynamic output bank supply current	LVDS Outputs; CM/LV = HIGH; V_{DD_nQ} = +3.6V; C_L = 40pF/output; R_L = 100Ω Differential	nQ[1:0] = 24MHz	--	0.5	mA/ Bank
			nQ[1:0] = 200MHz	--	3.5	
AI_{DD_XTAL} (Note 4)	Dynamic supply current from XTAL interface	XTAL_OUT Output V_{DD_C} = +3.6V; XTAL_IN = V_{DD_C} to V_{SS_R}; REF_SEL = LOW; RST/DIV = HIGH C_L = 40pF	REF = 2MHz PLL = 24MHz	--	1.5	mA
			REF = 50MHz PLL = 50MHz	--	2.0	

Notes:

* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1. When measuring the dynamic supply current, all outputs are disconnected from the equivalent test load defined in figure 8B.
2. To reduce power consumption for the device, the user may tie the unused V_{DD_nQ} pins to V_{SS_nQ}.
3. When measuring, use Figure 9.
4. Guaranteed by characterization, but not tested.

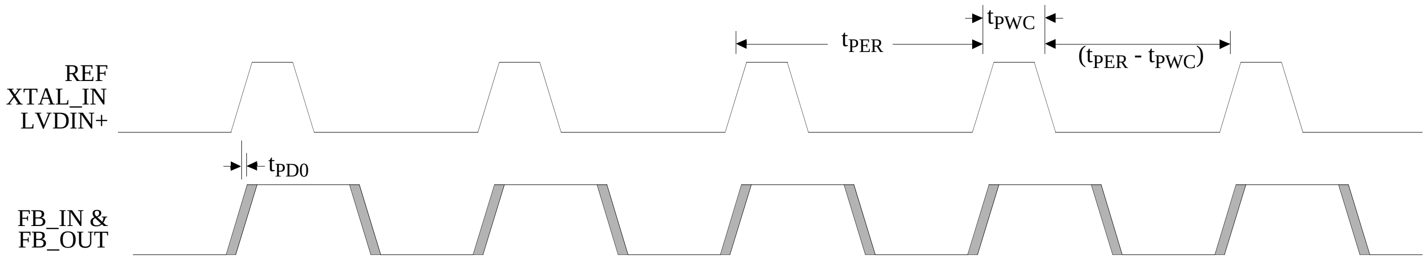

Figure 6a. Reference and Feedback Timing Diagrams

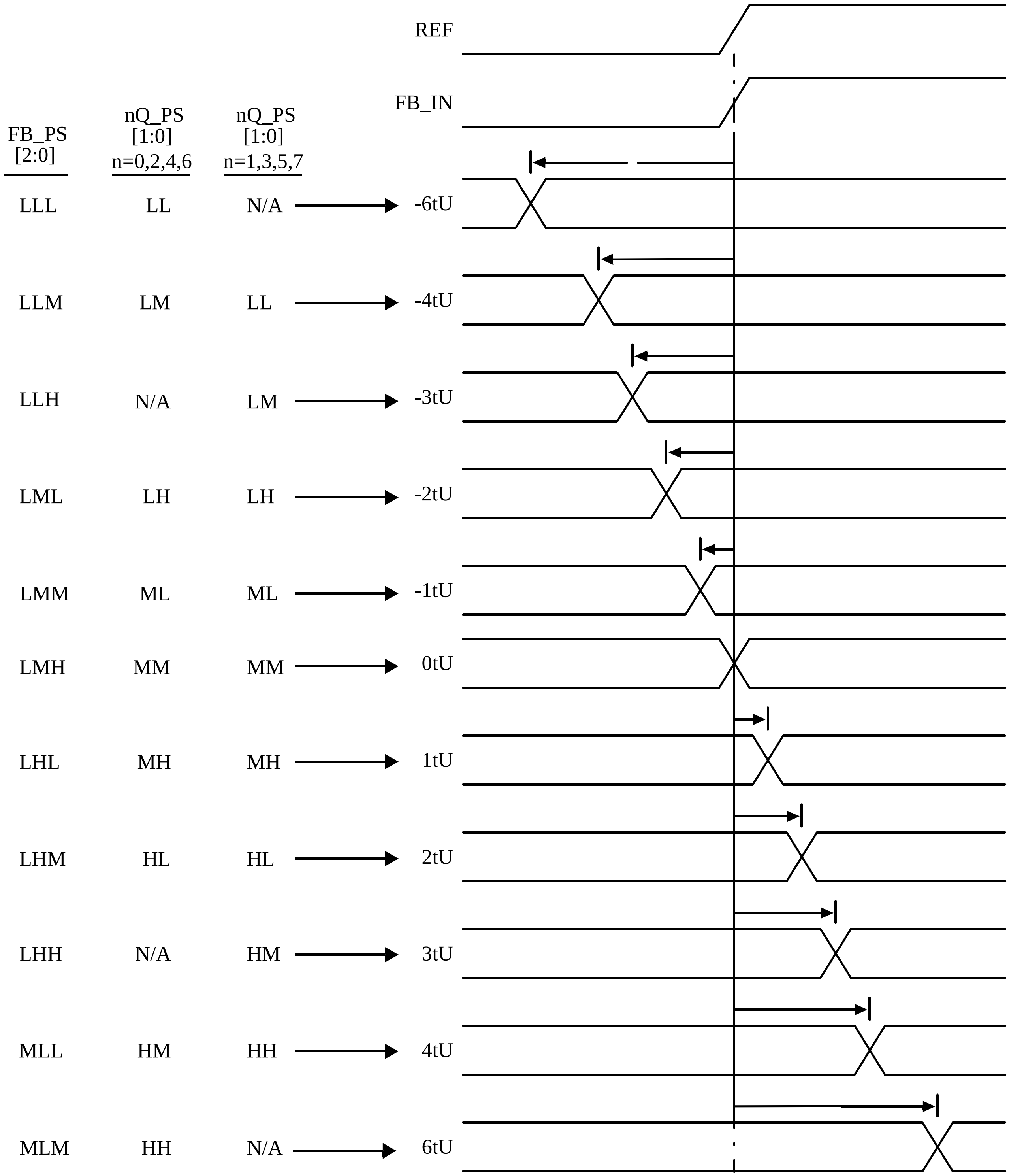

Figure 6b. Phase Select Time Unit Step Relationships

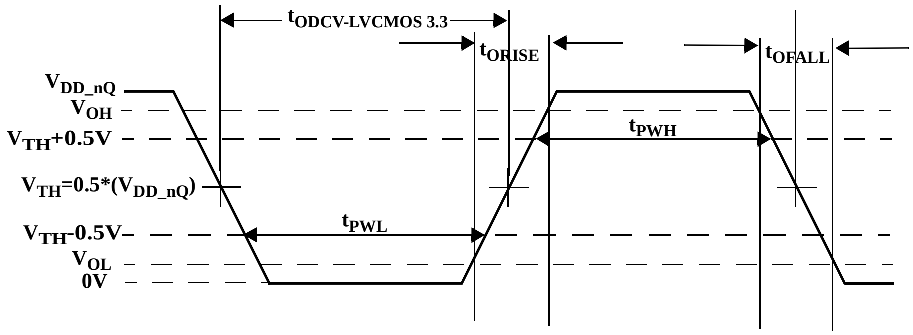

Figure 7A. +3.3V LVCMOS3.3/LVTTL Output Waveform

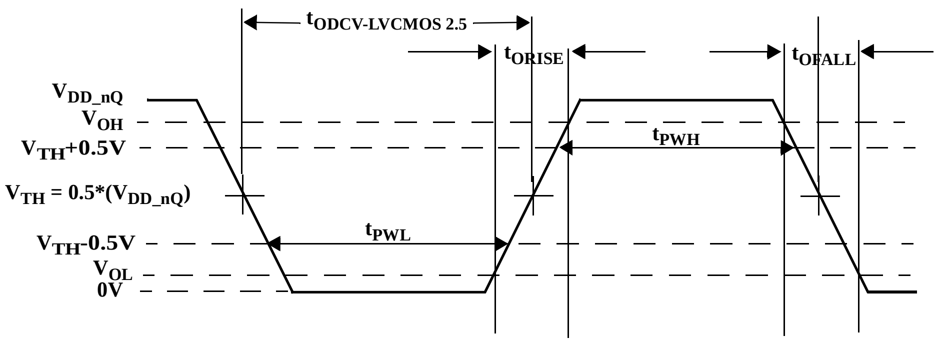

Figure 7B. +2.5V LVCMOS2.5/LVTTL Output Waveform

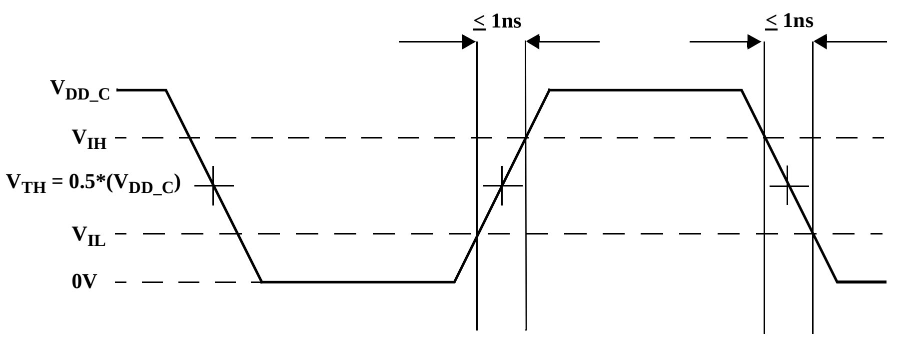

Figure 7C. LVCMOS3.3/LVTTL and XTAL_IN Input Test Waveform

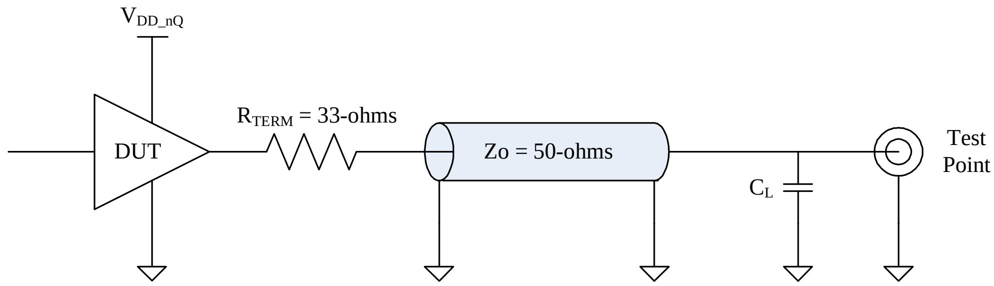

Figure 8A. Series Terminated LVCMOS/LVTTL Test Circuit

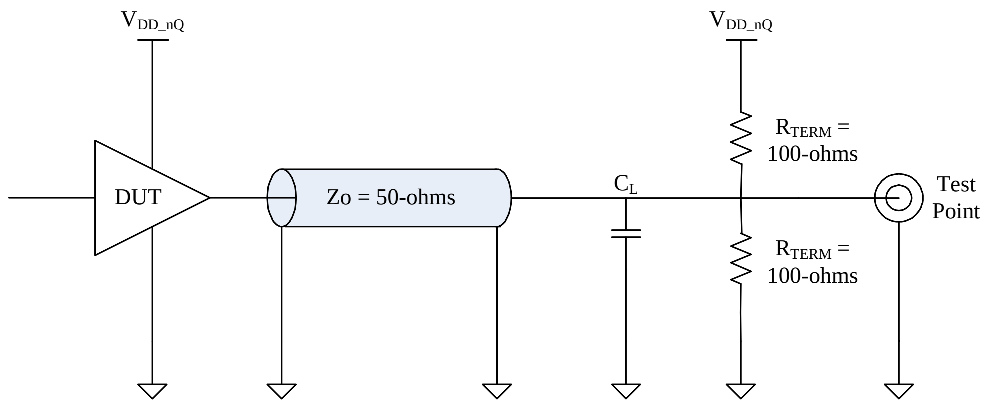

Figure 8B. Thevenin Terminated LVCMOS/LVTTL Test Circuit

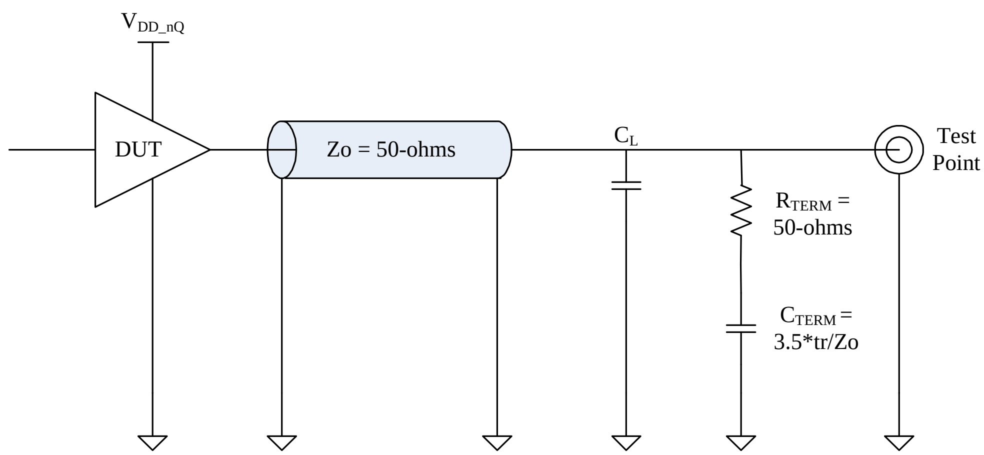

Figure 8C. AC Terminated LVCMOS/LVTTL Test Circuit

Note: For ATE test load, C_L=40pF. For lab characterization, C_L=15pF

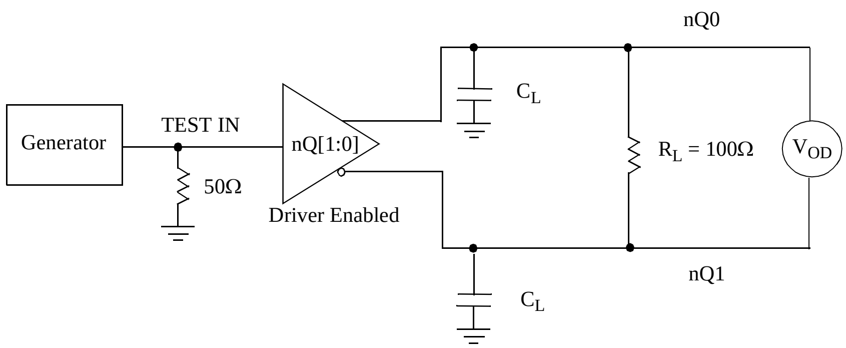

Figure 9. LVDS Driver V_{OD} and V_{OS} Test Circuit or Equivalent

Note: For ATE test load, C_L=40pF. For lab characterization, C_L=15pF

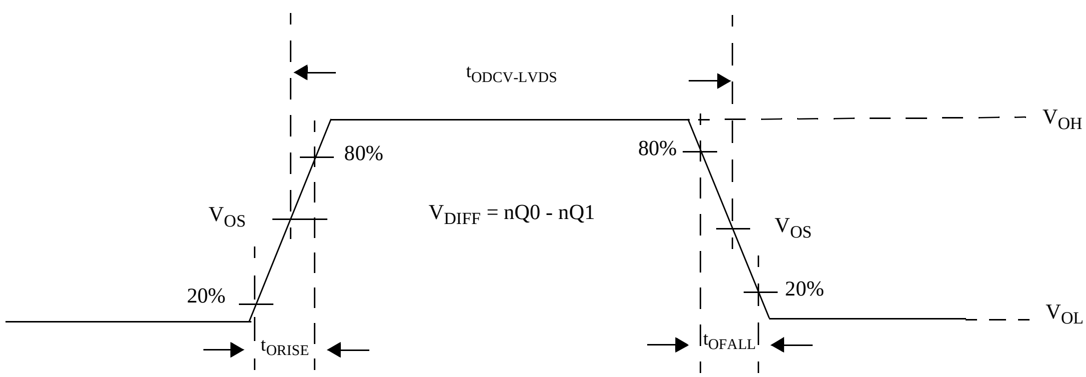

Figure 10. LVDS Driver Transition Time Waveform

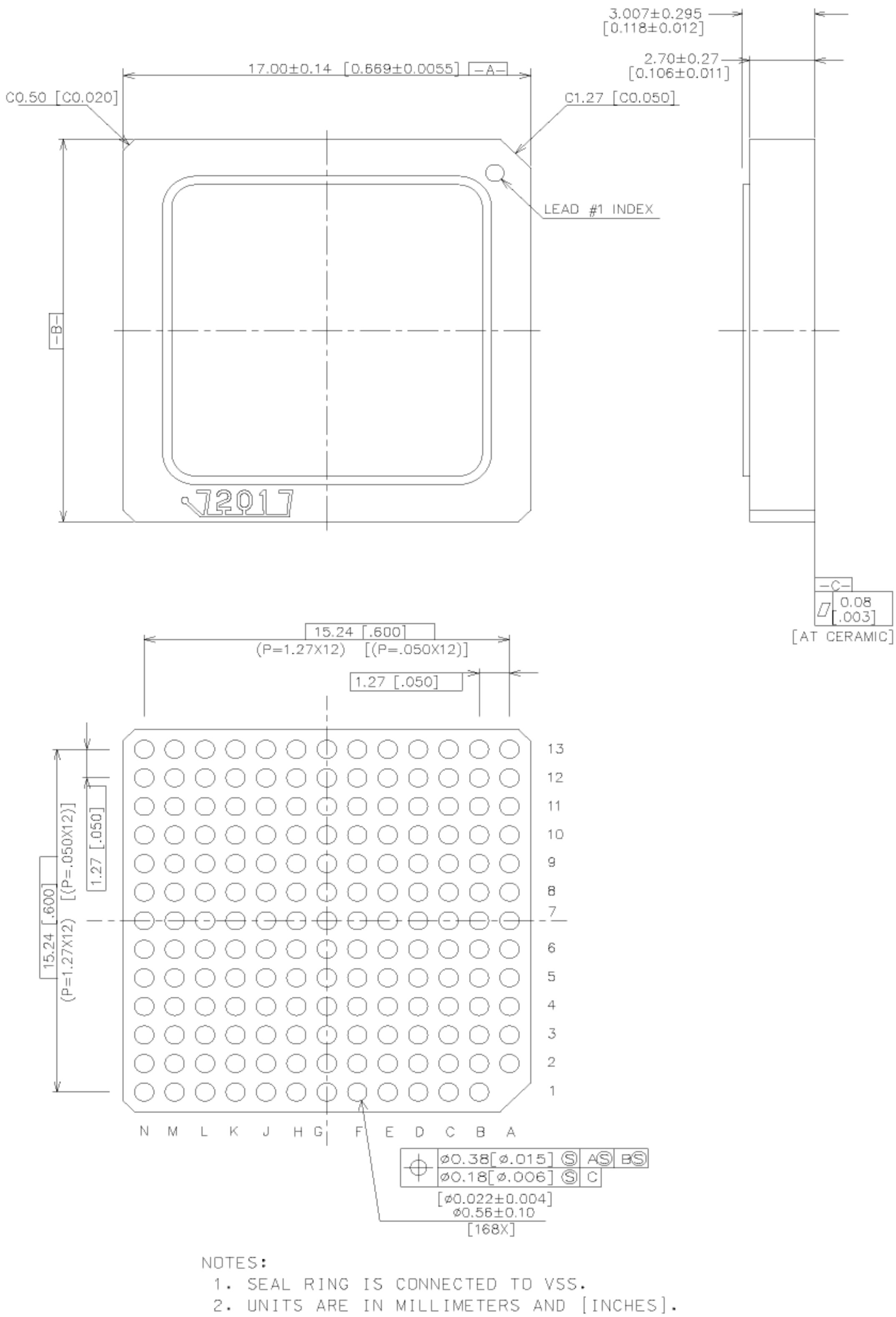

Figure 11. 168-CLGA Package

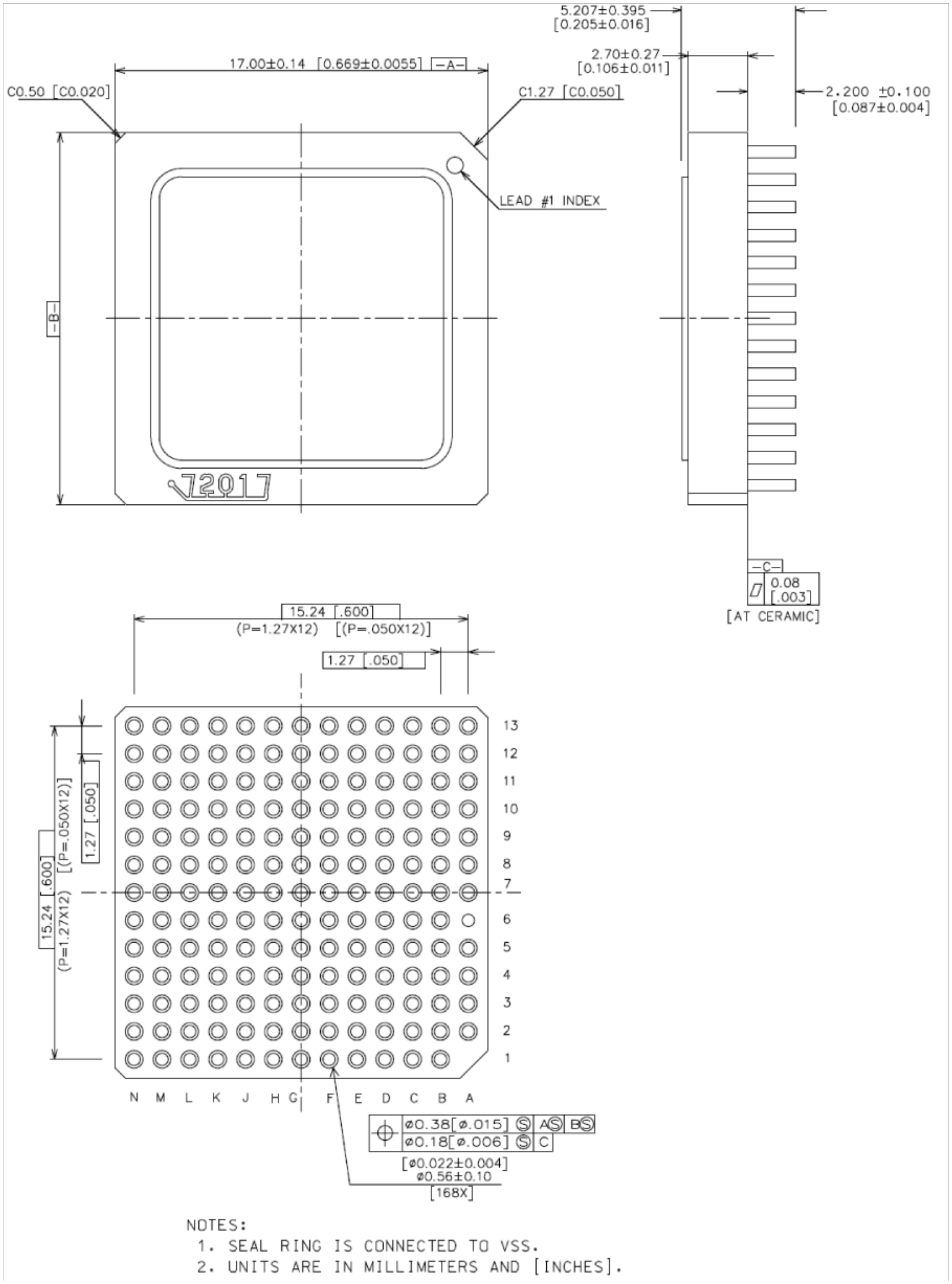

Figure 12. 168-CCGA Package

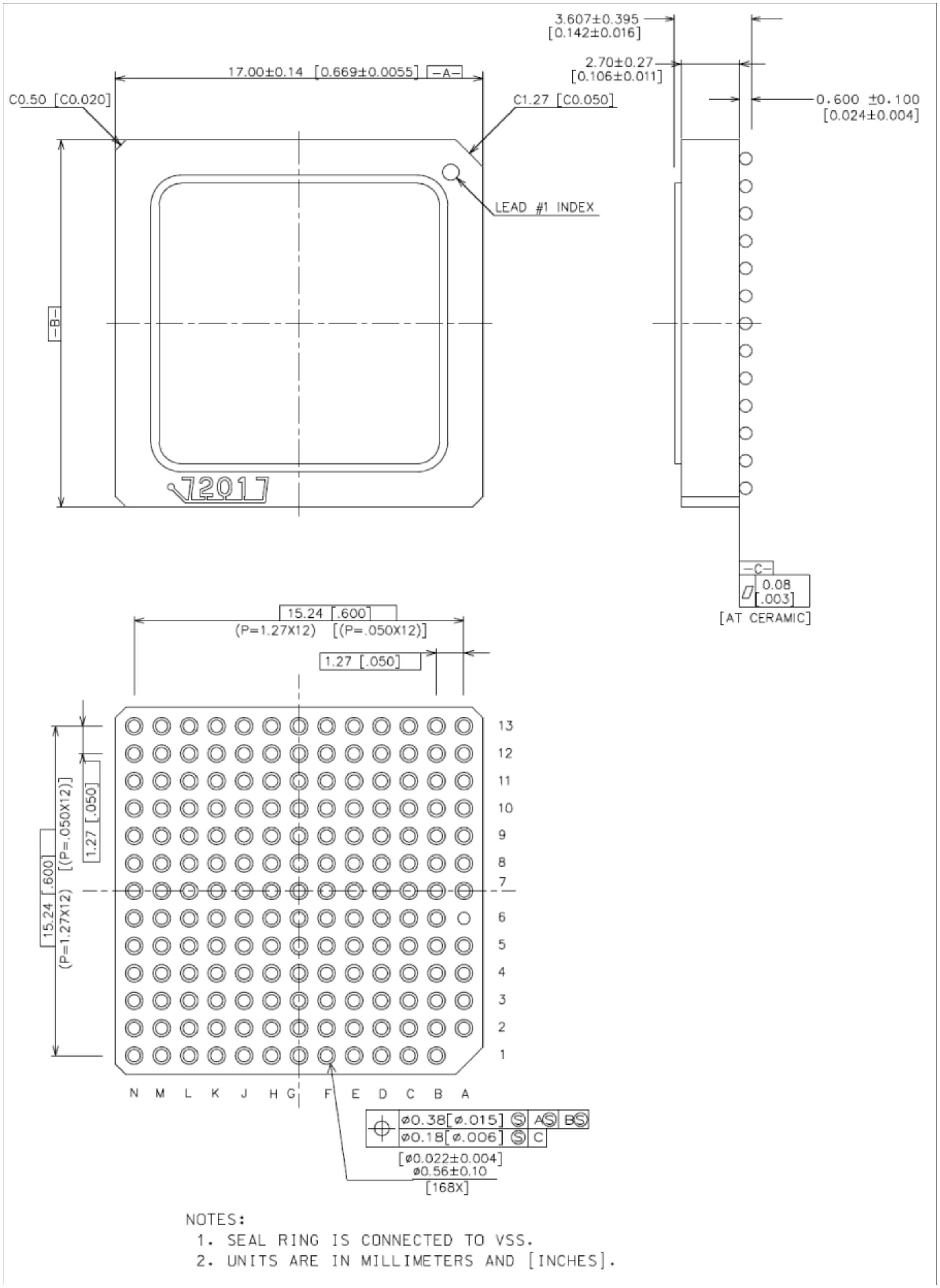

Figure 13. 168-CBGA Package

UT7R2XLR8 * * * * *

Lead Finish: **(Notes: 1)**
(A) = Hot Solder Dipped or Tinned
(C) = Gold

Screening Level: **(Notes: 2,3,4,5)**
(P) = Prototype Flow (Temperature Range: 25°C only)
(C) = HiRel Flow (Temperature Range: -55°C to +125°C)

Case Outline:
(Z) = 168-Ceramic Land Grid Array
(S) = 168-Ceramic Column Grid Array
(C) = 168-Ceramic Ball Grid Array (High Temp Solder Ball)

TID Tolerance:
(-) = None
(R) = 100 krad (Si)

Device Type
(16) = Clock Network Manager II with 16 clock outputs driven by eight clock banks

Generic UT7R2XLR8 part number

Notes:

1. Lead finish (A or C) must be specified.
2. Prototype Flow per Aeroflex Manufacturing Flows Document. Devices are tested at 25^{o}C only. Radiation is neither tested nor guaranteed.
3. HiRel Flow per Aeroflex Manufacturing Flows Document. Radiation TID tolerance may be ordered.

Package Option	Associated Lead Finish
(Z) 168 CLGA	**(C) Gold**
(S) 168 CCGA	**(A) Hot Solder Dipped**
(C) 168 CBGA	**(A) Hot Solder Dipped**

5962 * 08243 ** * * *

Lead Finish: **(Note 1)**
(C) = Gold
(A) = Solder

Case Outline:
(X) = 168-pin Ceramic Land Grid Array
(Y) = 168-pin Ceramic Column Grid Array

Class Designator:
(Q) = QML Class Q
(V) = QML Class V (Pending, contact Factory for availability)

Device Type: **(Note 2)**
01 = UT7R2XLR816 (Temperature Range: -55^{o}C to +125^{o}C)
02 = UT7R2XLR816 assembled to Aeroflex's Q+ flow (Temperature Range: -55^{o}C to +125^{o}C)

Drawing Number: **08243**

Total Dose:
(-) = none
(R) = 1E5 (100 krad (Si))

Federal Stock Class Designator: No options

Notes:
1. Lead finish is "C" (gold) only for case outline "X" and "A" (solder) only for cast outline "Y".
2. Aeroflex's Q+ assembly flow, as defined in section 4.2.2.d of the SMD, provides QML-Q product through the SMD that is manufactured with Aeroflex's standard QML-V flow, and has completed QML-V qualification per MIL-PRF-38535.

Aeroflex Colorado Springs - Datasheet Definition

Advanced Datasheet - Product In Development

Preliminary Datasheet - Shipping Prototype

Datasheet - Shipping QML & Reduced HiRel

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COBHAM

DATA SHEET REVISION HISTORY

REV	Revision Date	Description of Change	Author
1.0.0	4-15	Last official release	BM
1.0.1	10-15	Page 1 added Power dissipation bullet	BM
1.0.2	11-15	Page 1 added last two lines under Dedicated feedback Input/Output module bullet and added one line under Output clock bank signaling and control bullet. Added Cobham datasheet template.	BM
1.0.3	6-17	Page 1 and 46 removed Commercial and Industrial Temperature Ranges from datasheet and offering.	RT