Special Feature

Rad Hard, Space Ready

Case Study:

Evolution of a Fab-Independent Radiation-Hardened COTS IC Supplier

Even though rad-hard systems are essential in space and tactical military systems, rad-hard semiconductor processes are rare. But what's even more rare, is a fab-independent hardened process that can run in many COTS fabs.

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Strategic military and commercial space systems must survive and operate in severe ionizing radiation environments. In particular, strategic military systems must be uniquely hardened to survive a weapons-type burst of high-energy ionizing radiation. Although the exact radiation hardness requirements for military systems is not disclosed, it is known that these systems generally need hardening to prompt-type and total ionizing dose radiation, along with resistance to single-event upsets and latch-up. Similarly, commercial space systems must withstand the rigors of natural space and generally need hardening to total ionizing dose radiation, and resistance to single-event upsets and latch-up.

Although the need is great, the trouble has been the limited availability of radiation-hardened (rad-hard) semiconductor fabrication processes and facilities. Using the latest process technology available from commercial wafer foundries, Aeroflex UTMC has developed microelectronics that serve both strategic military and commercial space applications. The company's CRH module and proprietary design techniques for single-event latch-up and single-event effects mitigation, in combination with sub-micron and deep sub-micron mixed-signal process technology, allows for the develop-

Radiation-Hardened Requirement	Strategic Military System	Commercial Space System
Dose Rate Survivability	>$1x10^9$ rad(Si)/s	N/A
Dose Rate Upset	>$5x10^8$ rad(Si)/s	N/A
Survive accumulated total dose	>$5x10^5$ krad(Si)	100 to 300 krad(Si)
Charge particle strike induced upset	<$1x10^{-7}$ errors per bit day	<$1x10^{-7}$ errors per bit day
Immune to charge particle strike induced latch-up	>128 Me V-cm2/mg	>128 Me V-cm2/mg
Neutron Fluence (neutrons per centimeter squared)	$1x10^{14}$	N/A

Table 1

Typical Radiation Environment Requirements

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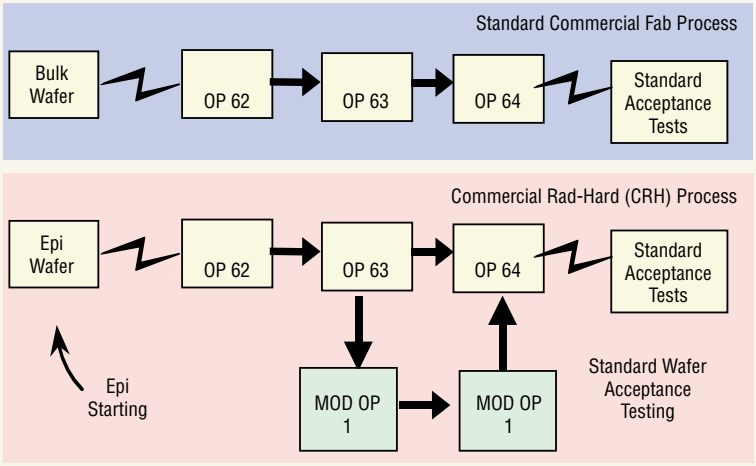

Figure 1

CRH process flow diagram, showing added steps (MOD OPs) that modify the commercial process flow operations.

ment of high-reliability microelectronics with state-of-the-art performance characteristics (high density, low power and high performance).

The company has qualified and shipped production rad-hard devices built using 0.6 µm and 0.25 µm design rules and is evaluating a 0.18 µm product that is consistent with the best-of-breed COTS IC fab processes. Table 1 describes the radiation-hardness requirements of strategic military and commercial space systems.

Benefits of Fab-Independence

Historically, both strategic and commercial radiation-hardened microelectronics have lagged commercial microelectronics in terms of speed, power and density since rad-hard microelectronics had to be fabricated in dedicated radiation-hardened silicon foundries running special processes. The extremely low total volume of rad-hard microelectronics generally made the pursuit of an aggressive leading-edge process technology roadmap (deep sub-micron) not a viable business proposition. In particular, this was a drawback for the satellite manufacturers who needed the capabilities of commercial microelectronics.

However, new and innovative advances in radiation hardening design/process intellectual property (IP), combined with the latest commercial processes (particularly thin-gate oxides, shallow trench isolation, and silicon-on-insulator), make it feasible to profitably manufacture strategic military and commercial space rad-hard microelectronics on par with the latest commercial technologies. Aeroflex UTMC solved the problem for the satellite manufacturers by using a "fab-independent" (also called "fabless") business model. Since 1996 commercial silicon has been successfully hardened from the effects of the natural and man-made (such as, weapon) space environment.

A fab-independent business model is not a new concept. In the commercial semiconductor market, leaders like Xilinix and Altera have taken market leadership positions using a similar business model. Free to seek the best technology for the application, fab-independent companies concentrate on product design and innovation, instead of fabrication plant construction and operation. Fab-independent companies are found to be flexible, viable and profitable. Typically, fab-independent companies are not financially bound to the multi-hundred million-dollar investments required to upgrade a wafer foundry either in wafer size (for example, from 200 mm to 300 mm) or critical dimension (for example, from 0.25 µm to 0.18 µm). They also leverage process and intellectual property (IP) of their commercial foundry partners, further reducing development costs and improving profitability.

The key initial phase of Aeroflex UTMC's switch from being an integrated circuit manufacturer building rad-hard CMOS products in a dedicated fabrication facility, to a fab-independent strategy was the development of the company's Commercial Rad-Hard (CRH) process module. The module utilized an existing commercial 0.6 µm CMOS wafer process minimizing development schedule and cost. The CRH process module was developed so that it was basically "minimally invasive;" that is, no process steps were changed or deleted.

Instead, a number of *proprietary* steps were added at one point in the baseline flow. Thus, for most of the wafer processing, both before and after the module insertion point, there is no distinction between rad-hard wafers and standard wafers. Satellite manufacturers require an assured supply; foundry relationships were formed with several dedicated commercial foundries, guaranteeing delivery of rad-hard products. Figure 1 shows the difference between a standard commercial process flow and that of the CRH flow.

Table 2 summarizes the radiation hardness results that have been achieved using this approach at AMI's fab in Pocatello, Idaho. Figure 2 and Figure 3 reflect the total dose performance of n-channel transistors with and without the CRH module via threshold voltage versus off-state tran-

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Radiation Effect	Levels	Comments
Total Ionizing Dose	100 krad(Si)–1 Mrad(Si)	The process module "recipe" can be adjusted to give different levels of total dose hardness.
Single-Event Upset	$1x10^{-8}$ – $1x10^{-10}$ errors/bit day	SEU is a function of the library cell. In general, the higher the SEU immunity, the larger the cell size.
Single-Event Latch-up	>100 MeV -cm^2/mg	Testing was performed at the 88" cyclotron at Lawrence Berkeley Lab
Prompt Dose Upset (Operate Through)	$4x10^8$ rad(Si)/s	A 20 ns pulse-width test was performed using the Boeing Radiation Effects Lab LINAC.
Prompt Dose Latch-up (Survivability)	>$3x10^{11}$ rad(Si)/s	A 35 ns pulse-width test was performed using the Boeing Radiation Effects Lab Flash X-ray.

Table 2
Summary of radiation hardness levels achieved on the Aeroflex UTMC 0.6 µm process.

Radiation Effect	Levels	Comments
Total Ionizing Dose	100 krad(Si)–1 Mrad(Si)	The process module "recipe" design rules and/or layout technique can be adjusted to give different levels of total dose hardness.
Single-Event Upset	$1x10^{-8}$ – $1x10^{-10}$ errors/bit day	SEU is a function of the library cell. In general, the higher the SEU immunity, the larger the cell size.
Single-Event Latch-up	>100 MeV -cm^2/mg	Testing was performed at the 88" cyclotron at Lawrence Berkeley Lab
Prompt Dose Upset (Operate Through)	$1x10^8$ rad(Si)/s	Estimated based on "good" design practices.
Prompt Dose Latch-up (Survivability)	>$1x10^{10}$rad(Si)/s	Estimated based on "good" design practices.

Table 3
Summary of radiation hardness levels achieved on the Aeroflex UTMC 0.25 µm process.

sistor leakage graphs. Transistors built with the CRH module show a 100x improvement in radiation tolerance, and are able to withstand greater than 300krad(Si) of ionizing dose before significant in-creases in intra-transistor leakage is observed. Gamma ray damage also impacts integrated circuits in the space environment (see sidebar: "Gamma Ray Damage").

A quick comparison of post-radiation transistor performance can be made by comparing I_d (drain current) of a standard N-channel transistor to that of a hardened N-channel transistor at V_g=0 volts. After exposure to 30 krads(Si), standard transistor leakage currents are upwards of 10 µA; the hardened transistor drain leakage is several nano-amps after exposure to 400 krads(Si). Again, satellite manufacturers requested validation of the CRH approach and the company was able to present no differences between dedicated fab produced rad-hard integrated circuits and fab-independent produced rad-hard integrated circuits.

Because of the rapid pace in commercial CMOS technology development, 0.25 µm became the next logical process to install the radiation hardening techniques (skipping 0.5 µm and 0.35 µm). In addition, preliminary

Aeroflex UTMC, formed in 1980, transitioned from a Qualified Manufacture List (QML) integrated circuit supplier with a dedicated fab to a QML "fab-independent" supplier of both rad-hard and non-hardened integrated microelectronics for aerospace and defense applications. With a fab-independent business model, the company subcontracts wafer manufacturing to pure-play wafer foundries. After the sale of its wafer fabrication facility, Aeroflex UTMC formed long-term relationships with leading edge wafer foundries. The result of the decision to use commercial fabrication facilities, combined with rad-hard process modules and/or design hardness techniques, was closure of the rad-hard/commercial technology gap, greatly expanding the number of rad-hard products available to satellite manufacturers.

The company's comprehensive digital and mixed-signal product portfolio is targeted for space applications with the goal of providing leading-edge integrated circuits for space-borne missions. For the rad-hard aerospace and defense marketplace, the company offers a wide range of products: digital CMOS ASIC technology (up to 3,000,000 gates), serial communication products (supporting bandwidths from 1 Mbit/s to 1.5 Gbits/s), complex and discrete logic, volatile and non-volatile memory and microcontroller products.

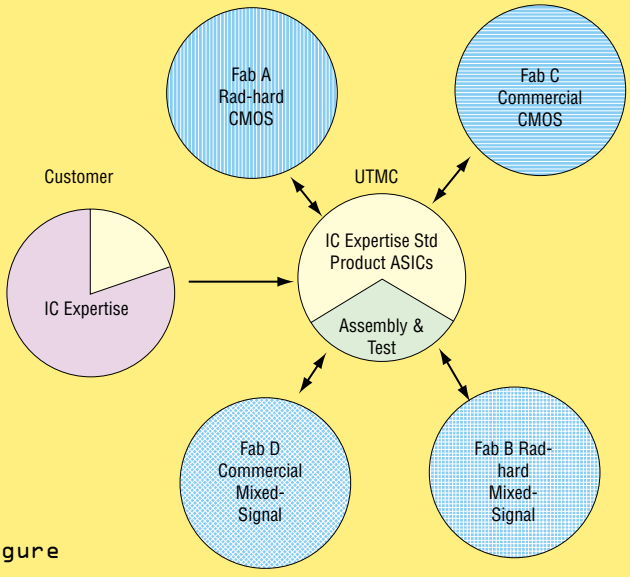

Figure
Aeroflex UTMC fab-independent (fabless) business model

Gamma Ray Damage

The absorption and interaction of gamma rays and x-rays with silicon is referred to as total dose. Gamma rays are members of the photon family that are quantized electromagnetic energy. Characterized by their wavelength, gamma and x-rays are considered waves of electromagnetic energy. High-energy gamma rays possess short wavelengths, on the order of fractions of an angstrom. Lower energy x-rays possess longer wavelengths of a few angstroms. Gamma and x-rays are a substantial portion of natural space environment, as well as the photon output of nuclear detonation. Gamma and x-rays have zero rest mass, their existence ceases when they are brought to rest. Photons travel at the speed of light, are uncharged and interact mainly with free electrons or electrons bound to an atomic system. Photon energy is described by the equation $E=hv=hc/\lambda$ where h is Planck's constant, c is the speed of light and λ is the wavelength on the incident photon.

Depending on their energy, x-rays and gamma rays interact with matter in three principal ways (Figure 1). The first is low energy x-rays on the order of a few KeV; their interactions are mainly through the Photoelectric Effect. X-rays penetrate the usually innermost electron shell structure of an atom; the excited atom expels one of its innermost electrons, thereby ionizing the atom. The expelled, swiftly moving electron carries off part of the energy supplied by the x-ray as kinetic energy.

Next, higher energy photons, namely in the energy regime of those emanating from a nuclear burst, interact with silicon via Compton Scattering. In this event, the x-ray photon scatters from the collision with less incident energy and excites the atom resulting in the expulsion of an electron. Finally, for very high-level photons, in the regime of gamma rays, a third interaction occurs called pair production (or pair creations). If the photon has sufficient energy the interaction results in generation of an electron and positron. The positron is a particle with all the properties of an electron, except that its charge is positive.

Whether the interaction is due to Photoelectric Effect, Compton Scattering or pair creation, the underlining effect that photon interaction has with silicon is the generation of electron-hole pairs as a result of energy absorption. In silicon, 4.0×10^{13} electron hole pairs are generated per cubic centimeter for each rad of energy absorbed, where one rad equals 100ergs per gram (or 3.6eV per electron). Ionization changes the silicon through the production of excess charged carriers and trapped charge in insulators. Electrons generated during the photon interaction are either swept out of the oxide due to electric fields or recombine with local atoms; holes remain in the oxide as trap sites and alter the silicon's intrinsic characteristics.

Trap sites within an insulator result in CMOS transistor threshold voltage shifts (V_T) and sneak paths for current flow. Figure 2 shows two common leakage paths occurring in leading-edge CMOS processes after exposure to ionizing dose. In the case of inter-device leakage, ionizing dose creates a channel underneath field oxides allowing current to flow between transistors that normally are isolated. Intra-transistor leakage results in the creation of a leakage path between transistors source and drain regions, this path can degrade transistor-switching performance and eventually leads to functional transistor failures. Transistor threshold voltage shifts are not as prevalent or worrisome in sub-micron and deep submicron processes due to the thin gate oxides used in conjunction with these processes. However, ionizing dose induced leakage paths do occur in these processes as a direct result of holes sites trapped in the oxide. Aeroflex UTMC CRH process technology was designed with great care to minimize these "sneak current" paths.

If ionization occurs over a short period of time, on the order of 20 to 50 ns, large photocurrents occur resulting in circuit anomalies. Circuits may exhibit logic-state upset due to supply rail upset (rail collapse), neutralization of charge stored on internal nodes or cells, or possible destructive latch-up or metal burnout. These phenomena are referred to as dose rate upset and dose rate latch-up, respectively. ■■

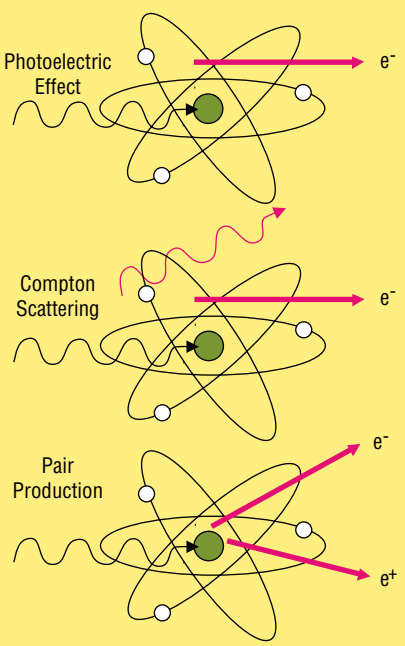

Figure 1

Gamma rays interact with silicon in three different ways: by ejecting an electron, a positron, a photon or a combination of each. Regardless, gamma rays disrupt the operation of a semiconductor device.

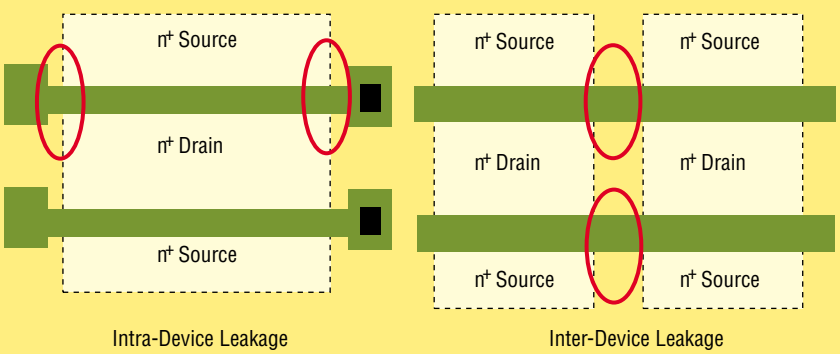

Figure 2

Gamma rays create electron-hole pairs that alter the intrinsic silicon device's performance by causing leakage paths. Intra-transistor leakage paths between transistor source and drain regions degrades transistor-switching performance and eventually leads to functional transistor failures. In the case of inter-device leakage, a channel is created underneath field oxides allowing current to flow between transistors that normally are isolated.

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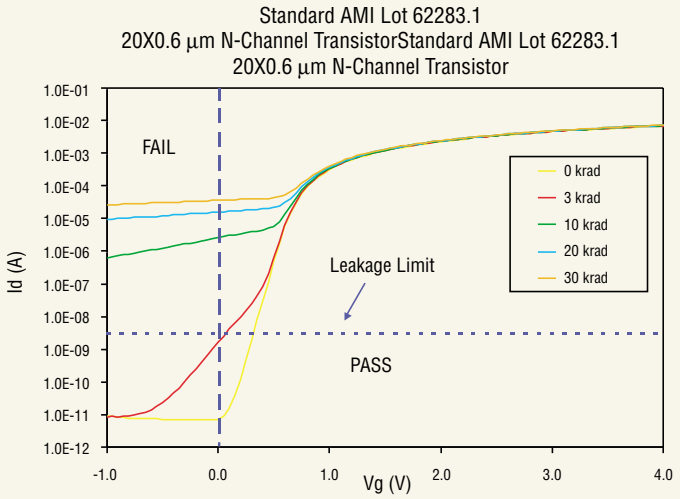

Figure 2

Drain current versus gate voltage. A standard transistor fails at approximately 3 krad(Si).

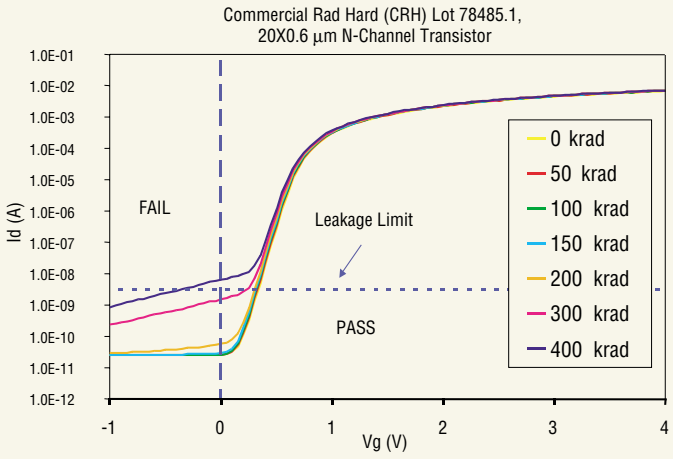

Figure 3

Drain current versus gate voltage. With the CRH process modifications, the transistor passes greater than 300 krad(Si).

experiments on the shallow trench isolation (STI) CMOS process manufactured at WaferTech, a Taiwan Semiconductor Microelectronics Corporation (TSMC) subsidiary in Camas, Washington, indicated that the Aeroflex UTMC *proprietary* process module approach could be integrated much more easily than it was on the 0.6 µm Localized Oxidation of Silicon (LOCOS) process. The 0.25 µm process module does not even require the manufacture of any additional masks. The final rad-hard process module at WaferTech consists of a combination of design rule modifications, transistor layout techniques and the re-use of certain masking levels at different points in the wafer fabrication process.

In this latter WaferTech/TSMC case, single-event upset and latch-up (SEU and SEL, respectively) immunity were achieved on the 0.25 µm process almost entirely through design hardness techniques. For SEU, Aeroflex UTMC experimented with many cell types to give the lowest bit-error rate while minimizing speed, power and area penalties. SEL hardness was achieved using the intrinsic tolerance of WaferTech's process (retrograde well technology) combined with layout techniques. Table 3 summarizes the radiation hardness results that have been achieved on a 0.25 µm process. It's important to note how the prompt dose upset and latch-up increases at the smaller geometry.

The COTS Approach Prevails

Although the conventional "wisdom" in the satellite industry said that a COTS-based fab-independent approach to serving the radiation-hardened market would surely fail, Aeroflex UTMC took the methodical approach to executing the fab-independent approach. To prove viability, the portable CRH module was installed at several wafer fabs. Renewable, multi-year foundry agreements were put in place to assure wafer supply. Test circuits were developed and processed for the sole purpose of collecting ionizing dose, single-event effects and reliability data for presentation to potential customers.

In addition, a family of storage cells (memory cells, flip-flops and latches) were designed that ranged from charge particle strike resistant to immune. Spatial design rules were developed to eliminate single- event latch-up and enhance ionizing dose and dose rate performance. In the end, convincing technical data supported the fab-independent business model. ▮▮

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