Synchronous SRAM (SSRAM) JTAG Operation

Table 1: Cross Reference of Applicable Products

Product Name:	Manufacturer Part Number	SMD #	Device Type	Internal PIC #
64Mbit Synchronous SRAM	UT8SP2M32	5962- TBD	All	WN05
64Mbit Synchronous SRAM	UT8SF2M32	5962-TBD	All	WN06

1.0 Overview

This application note defines the JTAG Serial Boundary Scan capability of the devices listed in Table 1.

2.0 Technical Background

Boundary scan is a method of verifying IC sub-blocks and circuit board to device lead integrity developed by JTAG (Joint Test Action Group) and standardized by IEEE 1149.1 in 1990.

2.1 JTAG Boundary Scan IEEE 1149.1

Table 1. defines the devices which incorporate a serial boundary scan test access port (TAP). The port operates in accordance with IEEE Standard 1149.1-1990 and supports the required instructions BYPASS, EXTEST, and SAMPLE/RPRELOAD, but does not contain complete set of functions required for full compliance to 1149.1. The TAP operates using JEDEC standard 3.3V I/O logic levels.

2.1.0 Enabling JTAG Boundary Scan

Device configuration per the applicable data sheet disables the JTAG boundary scan feature. Enabling the JTAG boundary scan feature requires the user drive device lead P16 (NUIH) LOW following proper power up requirements per the applicable device data sheet. The following sections describe the timing and characteristics of the JTAG Test Access Port (TAP). Aeroflex provides JTAG boundary scan operations through the TAP for lead integrity testing only in a terrestrial environment. Aeroflex does not recommend operation of the TAP in a radiation environment.

2.1.1 Test Access Port (TAP)

Test Clock (TCK)
The TAP controller Test Clock is only valid with the TAP controller. TCK registers all inputs on the rising edge and drives all outputs on the falling edge. When the TAP controller is not in use, TCK should remain a logic LOW through an externally connected 10Kohm pull-down resistor to VSSQ as indicated in the device data sheet.

Test MODE Select (TMS)
The TMS input provides commands to the TAP controller and is sampled on the rising edge of TCK. When TAP controller is not in use, TMS should remain a logic HIGH through an internally connected 75Kohm pull-up resistor to VDDQ as described in the device data sheet.

Test Data-In (TDI)
The TDI lead serially inputs information into the registers and can be connected to the input any register. The register between TDI and TDO is selectable by loading the applicable instruction into the TAP instruction register. For information about loading the instruction register, reference the TAP Controller State Diagram on page 6. When the TAP controller is not in use, TDI should remain a logic HIGH through an externally connected 10Kohm pull-up resistor to VDDQ as indicated in the device data sheet. TDI connects to the most significant bit (MSB) of any register (See the TAP Controller Block Diagram on page 7).

Test Data-Out (TDO)
The TDO output lead serially clocks data-out from the registers. The output is active depending upon the current state of the TAP state machine. The output changes on the falling edge of TCK. TDO connects to the least significant bit (LSB) of any register (see TAP Controller State Diagram on page 6). When the TAP controller is not in use, TDO should remain a logic HIGH through an externally connected 10Kohm pull-up resistor to VDDQ as indicated in the device data sheet.

2.1.2 TAP Instruction Set

The Three-bit TAP register recognizes four instructions. These instructions are BYPASS, EXTEST, PRELOAD, and SAMPLE (reference TAP Controller Codes Table 2).

EXTEST
EXTEST is a mandatory JEDEC 1149.1 instruction. Perform EXTEST by loading the instruction register with all ZEROs. This command supports board, package, and die-level continuity testing.

SAMPLE/PRELOAD
SAMPLE/PRELOAD is a 1149.1 mandatory instruction. The PRELOAD portion of this instruction is not available. Loading the SAMPLE/PRELOAD instruction into the instruction register while the TAP controller is in the Capture-DR state captures a snapshot of the data on the inputs and bidirectional leads in the boundary scan register.

BYPASS
Loading the instruction register with the BYPASS instruction while the TAP is in Shift-DR state, places the bypass register between TDI and TDO leads. The advantage of the BYPASS instruction is that it shortens the boundary scan path when connecting multiple devices together on a board.

2.1.2.1 TAP Controller Codes

Table 2: TAP Controller Identification Codes

Instruction	Code	Description
EXTEST	000	Performs boundary scan test. This instruction is not fully 1149.1 compliant as bi-directs are not fully controllable via JTAG but are forced into input mode.
SAMPLE/PRELOAD	100	PRELOAD portion of this instruction is not available; therefore, the instruction is not fully 1149.1 compliant
BYPASS	111	Places bypass register between TDI and TDO. BYPASS instruction shortens boundary scan path for multiple part testing

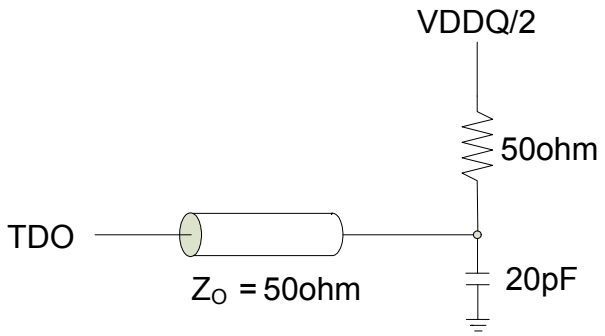
3.0 TAP Controller Specifications

The following subsections outline the TAP AC and DC Test Conditions, State Diagram, Block Diagram, DC and AC Characteristics, TAP Timing Diagram, and Boundary Scan Exit Order.

3.1.0 2.5V and 3.3V TAP AC Test Conditions

Input voltage levels.....VDDQ to 2.5V or 3.3V
Input pulse levels.....VSS to VDDQ
Input rise and fall times..... 1 ns
Input timing reference levels.....VDDQ/2 (V)
Output reference levels.....VDDQ/2 (V)
Test load termination supply voltage.....VDDQ/2 (V)

TAP Output Load Equivalent



3.1.1 TAP AC Characteristics

Table 3: TAP AC Switching Characteristics
(25°C Only; VDD = 3.3V +/- 0.3V unless otherwise noted)[1,2]

Parameter	Description	Min	Max	Unit
Clock				
t_{TCYC}	TCK Clock Cycle Time	100		ns
t_{TF}	TCK Clock Frequency		10	MHz
t_{TH}	TCK Clock HIGH Time	40		ns
t_{TL}	TCK Clock LOW Time	40		ns
Output Times				
t_{TDOV}	TCK Clock LOW to TDO Valid		20	ns

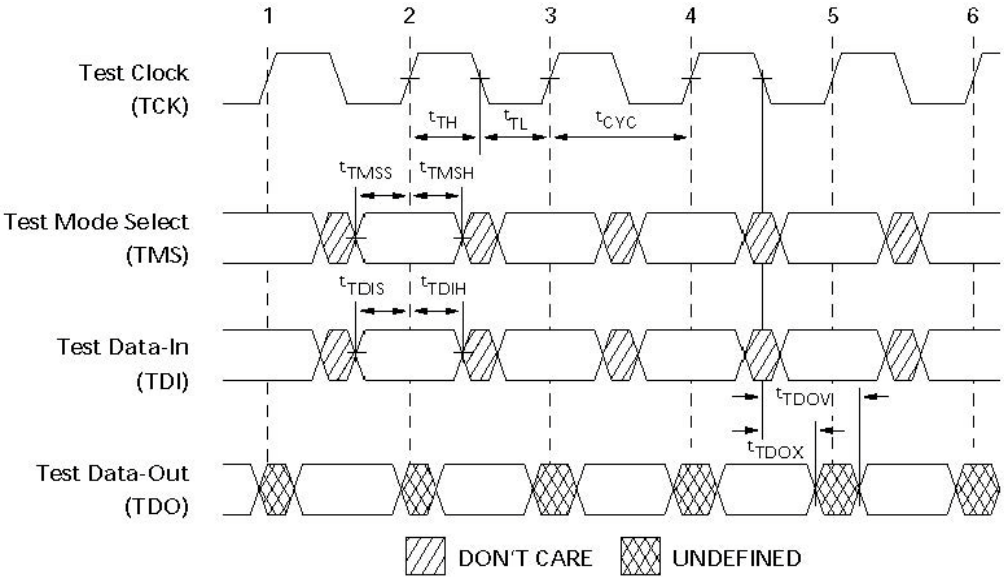
Table 3: TAP AC Switching Characteristics

(25°C Only; VDD = 3.3V +/- 0.3V unless otherwise noted)[1,2]

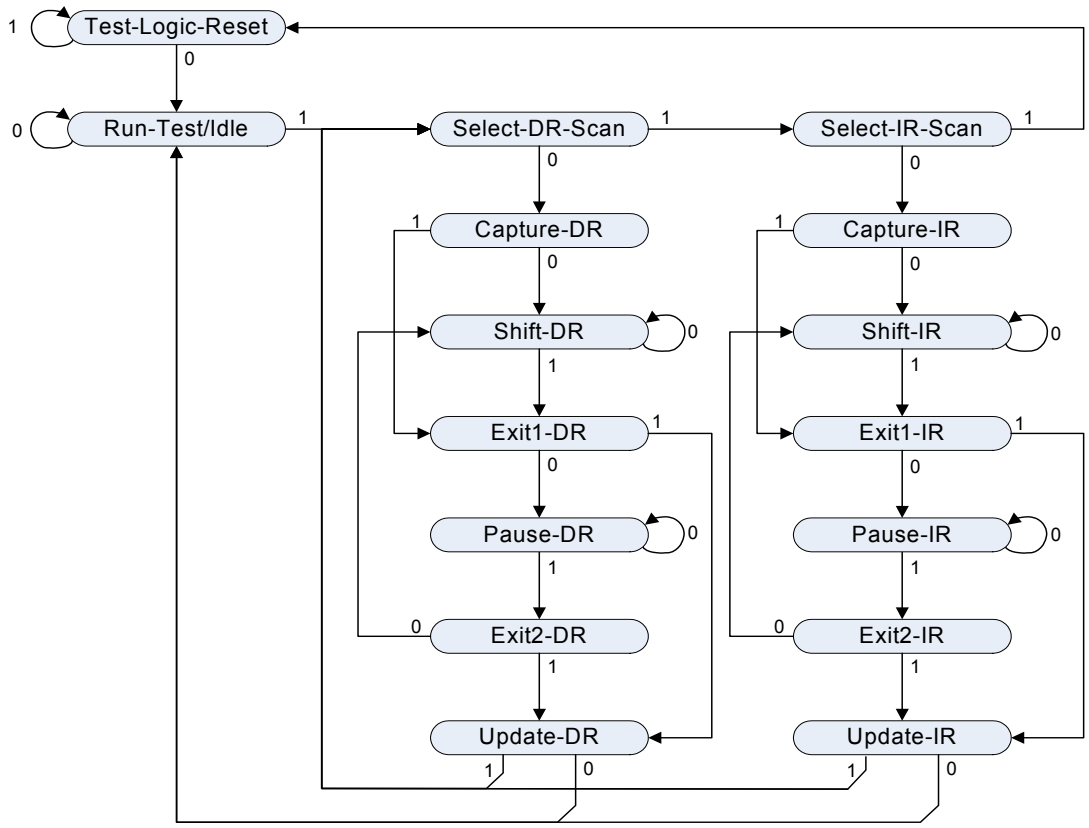
t_{TDOX}	TCK Clock LOW to TDO Invalid	0		ns
Set-up Times				
t_{TMSS}	TMS Set-up to TCK Clock Rise	10		ns
t_{TDIS}	TDI Set-up to TCK Clock Rise	10		ns
t_{CS}[3]	Capture Set-up to TCK Rise	10		ns
Hold Times				
t_{TMSH}	TMS Hold after TCK Clock Rise	10		ns
t_{TDIH}	TDI Hold after TCK Clock Rise	10		ns
t_{CH}[3]	Capture Hold after TCK Clock Rise	10		ns

Notes:
1. Characteristics are specified using input and load conditions in paragraph 3.1.0
2. Guaranteed by design
3. T_{CS} and T_{CH} refer to setup and hold requirements for latching data from the boundary scan register.

TAP Timing Diagram



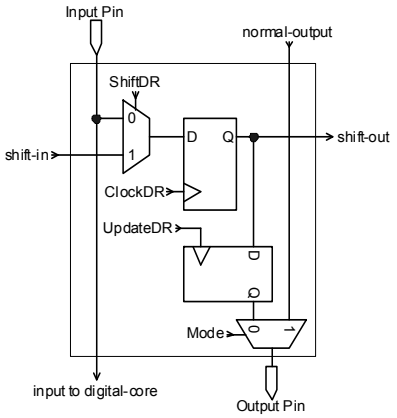
3.1.2 TAP Controller State Diagram

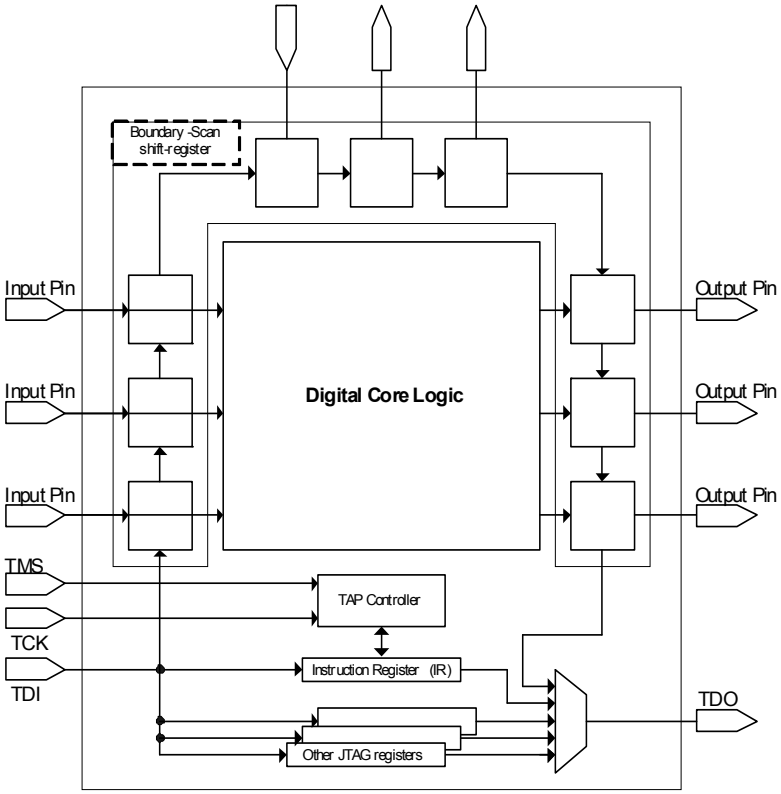


Notes:

1. All state transitions for the TAP Controller occur based on the value of TMS at the rising edge of TCK

3.1.3 TAP Controller Block Diagram





Notes:

1. Input Pin and Output Pin are only applicable if specific cell-bit captures Input Pin or updates/drives Output Pin, respectively.
2. Shift-in comes from previous cell-bit in DR shift register.
3. Shift-out feeds to next cell-bit in DR shift-register.
4. ClockDR is active for both Shift-DR and Capture-DR commands.
5. UpdateDR is only active for Update-DR commands.
6. ShiftDR is 0 only for Capture-DR commands.
7. Normal-output is the (non-JTAG) output from the on-chip digital-core per normal functional operation.
8. Mode is 0 only if the IR command equals EXTEST.
9. Input to digital-core is the (non-JTAG) input to the on-chip digital-core per normal functional operation.

3.1.4 TAP Controller Boundary Scan Order

Table 5: Boundary Scan Exit Order

TDI & TDO Order (LSb-first)	I/O Name	Device Pin Designator	Access Mode	Comments
0	Logic Zero	R8	External Level Capture	Reserved
1	Logic Zero	R7	External Level Capture	Reserved
2	Logic Zero	P9	External Enable Force (Always captures “0”)	Active-high output-enable.
3	Logic Zero	P9	External Level Force (Always captures “0”)	
4	EDACEN	P16	External Level Capture	
5	DQ[51]	N1	External Level Capture	External Force of DQ[]’s not supported
6	DQ[49]	N2	External Level Capture	External Force of DQ[]’s not supported
7	DQ[47]	M2	External Level Capture	External Force of DQ[]’s not supported
8	DQ[45]	M1	External Level Capture	External Force of DQ[]’s not supported
9	DQ[43]	M3	External Level Capture	External Force of DQ[]’s not supported
10	DQ[41]	L2	External Level Capture	External Force of DQ[]’s not supported
11	DQ[31]	L1	External Level Capture	External Force of DQ[]’s not supported
12	DQ[29]	L3	External Level Capture	External Force of DQ[]’s not supported
13	DQ[27]	K1	External Level Capture	External Force of DQ[]’s not supported
14	DQ[25]	K2	External Level Capture	External Force of DQ[]’s not supported
15	DQ[23]	K3	External Level Capture	External Force of DQ[]’s not supported
16	DQ[21]	J3	External Level Capture	External Force of DQ[]’s not supported
17	DQ[19]	J1	External Level Capture	External Force of DQ[]’s not supported
18	DQ[17]	J2	External Level Capture	External Force of DQ[]’s not supported
19	MBE1	H1	External Enable Force (Always captures “0”)	Active-high output-enable.
20	MBE1	H1	External Level Force (Always captures “0”)	
(SW-quadrant of BSCAN-chain ends, NW-quadrant begins)				
21	DQ[15]	H2	External Level Capture	External Force of DQ[]’s not supported
22	DQ[13]	G3	External Level Capture	External Force of DQ[]’s not supported
23	DQ[11]	G2	External Level Capture	External Force of DQ[]’s not supported
24	DQ[9]	G1	External Level Capture	External Force of DQ[]’s not supported
25	DQ[7]	F3	External Level Capture	External Force of DQ[]’s not supported
26	DQ[5]	F2	External Level Capture	External Force of DQ[]’s not supported
27	DQ[3]	F1	External Level Capture	External Force of DQ[]’s not supported
28	DQ[1]	E2	External Level Capture	External Force of DQ[]’s not supported
29	DQ[39]	E3	External Level Capture	External Force of DQ[]’s not supported
30	DQ[37]	E1	External Level Capture	External Force of DQ[]’s not supported
31	DQ[35]	D2	External Level Capture	External Force of DQ[]’s not supported
32	DQ[33]	D1	External Level Capture	External Force of DQ[]’s not supported
33	LOGIC ZERO	NA[1]	External Level Capture	Reserved
34	LOGIC ZERO	NA[1]	External Level Capture	Reserved

Table 5: Boundary Scan Exit Order

35	READY	C4	External Enable Force (Always captures "0")	Active-high output-enable.
36	READY	C4	External Level Force (Always captures "0")	
37	FLSH_PIPE	C5	External Level Capture	
38	LOGIC ZERO	C6	External Level Capture	
39	LOGIC ZERO	A6	External Level Capture	Reserved
40	/OE	B4	External Level Capture	Effect on DQ[] & MBE0/1/C is disabled during EXTEST.
41	LOGIC ZERO	B5	External Level Capture	Reserved
42	/CS2	A4	External Level Capture	
43	/WE	A5	External Level Capture	
44	ADDR[11]	B6	External Level Capture	
45	ADDR[10]	A7	External Level Capture	
46	ADDR[9]	B7	External Level Capture	
47	ADDR[8]	A8	External Level Capture	
48	ADDR[7]	C7	External Level Capture	
49	ADDR[6]	B8	External Level Capture	
50	ADDR[5]	C8	External Level Capture	
51	ADDR[4]	A9	External Level Capture	
52	/CEN	H3	External Level Capture	
(NW-quadrant of BSCAN-chain ends, NE-quadrant begins)				
53	CLK	H18	External Level Capture	
54	ADDR[17]	B9	External Level Capture	
55	ADDR[18]	A10	External Level Capture	
56	ADDR[20]	B11	External Level Capture	
57	ADDR[19]	A11	External Level Capture	
58	ADDR[16]	B12	External Level Capture	
59	ADDR[13]	B13	External Level Capture	
60	ADDR[14]	A12	External Level Capture	
61	ADDR[15]	A13	External Level Capture	
62	ADDR[12]	B14	External Level Capture	
63	ADDR[3]	C15	External Level Capture	
64	ADDR[2]	A14	External Level Capture	
65	ADDR[1]	B15	External Level Capture	
66	ADDR[0]	A15	External Level Capture	
67	ADV_LDb	C16	External Level Capture	
68	CS1	C17	External Level Capture	
69	LOGIC ZERO	NA[1]	External Level Capture	Reserved
70	/CS0	A16	External Level Capture	
71	LOGIC ZERO	NA[1]	External Level Capture	Reserved
72	ZZ	B16	External Level Capture	
73	LOGIC ZERO	B17	External Level Capture	Reserved
74	LOGIC ZERO	A18	External Level Capture	Reserved

Table 5: Boundary Scan Exit Order

75	LOGIC ZERO	A17	External Level Capture	Reserved
76	SHUTDOWN	B18	External Level Capture	
77	LOGIC ZERO	NA[1]	External Level Capture	Reserved
78	DQ[32]	D20	External Level Capture	External Force of DQ[]'s not supported
79	DQ[34]	E20	External Level Capture	External Force of DQ[]'s not supported
80	DQ[36]	E19	External Level Capture	External Force of DQ[]'s not supported
81	DQ[38]	E18	External Level Capture	External Force of DQ[]'s not supported
82	DQ[0]	F19	External Level Capture	External Force of DQ[]'s not supported
83	DQ[2]	F20	External Level Capture	External Force of DQ[]'s not supported
84	DQ[4]	F18	External Level Capture	External Force of DQ[]'s not supported
85	DQ[6]	G19	External Level Capture	External Force of DQ[]'s not supported
86	DQ[8]	G20	External Level Capture	External Force of DQ[]'s not supported
87	DQ[10]	G18	External Level Capture	External Force of DQ[]'s not supported
88	DQ[12]	H19	External Level Capture	External Force of DQ[]'s not supported
89	DQ[14]	J18	External Level Capture	External Force of DQ[]'s not supported
(NE-quadrant of BSCAN-chain ends, SE-quadrant begins)				
90	MBE0	H20	External Enable Force (Always captures "0")	Active-high output-enable.
91	MBE0	H20	External Level Force (Always captures "0")	
92	DQ[16]	J19	External Level Capture	External Force of DQ[]'s not supported
93	DQ[18]	J20	External Level Capture	External Force of DQ[]'s not supported
94	DQ[20]	K18	External Level Capture	External Force of DQ[]'s not supported
95	DQ[22]	K20	External Level Capture	External Force of DQ[]'s not supported
96	DQ[24]	K19	External Level Capture	External Force of DQ[]'s not supported
97	DQ[26]	L18	External Level Capture	External Force of DQ[]'s not supported
98	DQ[28]	L20	External Level Capture	External Force of DQ[]'s not supported
99	DQ[30]	L19	External Level Capture	External Force of DQ[]'s not supported
100	DQ[40]	M18	External Level Capture	External Force of DQ[]'s not supported
101	DQ[42]	M20	External Level Capture	External Force of DQ[]'s not supported
102	DQ[44]	M19	External Level Capture	External Force of DQ[]'s not supported
103	DQ[46]	N18	External Level Capture	External Force of DQ[]'s not supported
104	DQ[48]	N19	External Level Capture	External Force of DQ[]'s not supported
105	DQ[50]	N20	External Level Capture	External Force of DQ[]'s not supported
106	LOGIC ZERO	R16	External Level Capture	Reserved
107	SCRUBEN	P5	External Level Capture	
108	FREQSEL	R14	External Level Capture	
109[2]	LOGIC ONE	R13	External Level Capture	UT8SP2M32 OPTION (NOTE 2)
109[2]	LOGIC ZERO	R13	External Level Capture	UT8SF2M32 OPTION (NOTE 2)
110	MODE	P12	External Level Capture	
111	LOGIC ONE	R11	External Level Capture	Reserved
112	MBEC	R10	External Enable Force (Always captures "0")	Active-high output-enable.

Table 5: Boundary Scan Exit Order

113	MBEC	R10	External Level Force (Always captures "0")	

NOTES:
1. The boundary scan register order position is internally connected to indicated state and is not accessible through an external connection.
2. The boundary scan register order is specific for indicated device typed.

4.0 Summary and Conclusion

The devices in Table 1 incorporate a serial boundary scan test access port (TAP). The port operates in accordance with IEEE Standard 1149.1-1990 and supports required instructions BYPASS, EXTEST, and SAMPLE/PRELOAD, but does not contain the complete set of functions required for full compliance to 1149.1. The TAP operates using JEDEC standard 3.3V or 2.5V I/O logic levels.

Contained herein are the following TAP controller specifications:

TAP Controller Identification Codes
TAP AC Switching Characteristics
TAP Timing Diagram
TAP Controller State Diagram
TAP Controller Block Diagram
TAP Controller Boundary Scan Exit Order