

LEON 3FT Memory Configuration

Table 1: Cross Reference of Applicable Products

Product Name:	Manufacturer Part Number	SMD #	Device Type	Internal PIC
LEON 3FT	UT699	5962-08228	ALL	WG07

1.0 Overview

This application note describes how to use the LEON 3FT memory configurations spreadsheet. The spreadsheet is to help assist on setting up memory configuration registers 1, 2 and 3 and is located at <http://www.aeroflex.com/leon>

- Use memory configuration register 1 to program the timing of the ROM and I/O accesses.
- Use memory configuration register 2 to control the timing for the SRAM and SDRAM.
- Memory configuration register 3 contains the reload value for the SDRAM refresh counter and to control/monitor the memory EDAC. It also contains the configuration of the register file EDAC.

Table 2: FTMCTRL Memory Controller Registers

REGISTER	APB ADDRESS
Memory Configuration register 1 (MCFG1)	0x80000000
Memory Configuration register 2 (MCFG2)	0x80000004
Memory Configuration register 3 (MCFG3)	0x80000008

2.0 LEON3FT Memory Configuration

The memory configuration spreadsheet has four different worksheets, MCFG1, MCFG2, MCFG3, and Calculations. To calculate the memory configuration registers, input a binary ('1' or '0') in the *Value (binary)* column. All the fields that have *Res* in the *Name* field are reserved. Also, in MCFG1 the PZ field (size of each PROM bank) is reserved as the UT699 has a fixed PROM bank size. As the values are inserted, the MCFG's are updated. See the (*UT699 LEON3FT Functional Manual*) to see how to configure each bit in the memory configuration registers.

31	30	29	28	27	26	25	24	23	20	19	18	17	14	13	12	11	10	9	8	7	4	3	0
--	PB	AB	IW	IB	BE	--		IW	IE	--		PZ	---	PE	--	PD		PW					PR

Leon 3 Memory Configuration Register 1

Bit Number	Name	Value (binary)
31	Res	0
30	PB	0
29	AB	0
28-27	IW	1 0
26	IB	0
25	BE	0
24	Res	0
23-20	IW	0 1 1 1
19	IE	1
18	Res	0
17-14	PZ	1 1 1 1
13-12	Res	0 0
11	PE	0
10	Res	0
9-8	PD	1 0
7-4	PW	1 1 1 1
3-0	PR	1 1 1 1

	PB	AB	IW	IB	BE	IW	IE	PZ	PE	PD	PW	PR																				
MCFG1	Reserved	Prom area bus enable	Asynchronous bus ready	I/O data bus width	I/O area bus ready enable	Bus error enable	Reserved	Number of waitstates during I/O accesses	I/O enable	Reserved	Size of each PROM bank (hardwired to 0xF)	Reserved	Prom write enable	Reserved	Data width of the Prom area	Number of waitstates during PROM write cycles	Number of waitstates during PROM read cycles															
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	1	0	0	0	0	0	1	1	1	1	0	1	1	1	1	0	0	0	0	1	0	1	1	1	1	1	1	1	1
		1				0		7		B		C									2				F					F		

MCFG1 = 0x107BC2FF

Figure 1: Memory Configuration Register 1

31	30	29	27	26	25	23	22	21	20	19	18	17	16	15	14	13	12	9	8	7	6	5	4	3	2	1	0
DR	DP	DF	DC	DZ	DS	DD	BW	--	DE	SI	SZ	--	SB	RM	SD	SW	SR										

Leon 3 Memory Configuration Register 2

Bit Number	Name	Value (binary)
31	DR	1
30	DP	0
29-27	DF	0 1 0
26	DC	0
25-23	DZ	1 0 0
22-21	DS	0 1
20-19	DD	0 0
18	BW	0
17-15	Res	0 0 0
14	DE	1
13	SI	0
12-9	SZ	1 0 1 0
8	Res	0
7	SB	0
6	RM	1
5-4	SD	1 0
3-2	SW	0 0
1-0	SR	0 0

	DR	DP	DF	DC	DZ	DS	DD	BW	DE	SI	SZ	SB	RM	SD	SW	SR																	
MCFG2	SDRAM refresh	SDRAM TRP parameter	SDRAM TRFC parameter	SDRAM CAS Parameter	Bank Size for SDRAM chip selects	SDRAM column size	SDRAM command	Memory cntrlr bus width	Reserved	SDRAM enable	SRAM disable	Size of each SRAM bank	Reserved	SRAM bus ready enable	Enable Read-modify-write	Data width of SRAM area	Number of waitstates during SRAM write cycles	Number of waitstates during SRAM read cycles															
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	1	0	0	1	0	0	1	0	0	0	1	0	0	0	0	0	0	1	0	1	0	1	0	0	0	1	1	1	0	0	0	0	0
		9			2			2			0		5			4				6									0				

MCFG2 = 0x92205460

Figure 2: Memory Configuration Register 2

31	30	29	28	27	26	11	10	9	8	7	0
RFC	--	ME	RLDVAL			WB	RB	SE	PE	TCB [7:0]	

Leon 3 Memory Configuration Register 3

Bit Number	Name	Value (binary)
31-28	Res	0 0 0 0
27	ME	1
26-12	RLDVAL	0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 1
11	WB	0
10	RB	0
9	SE	0
8	PE	0
7-0	TCB	0 0 0 0 0 0 0 0

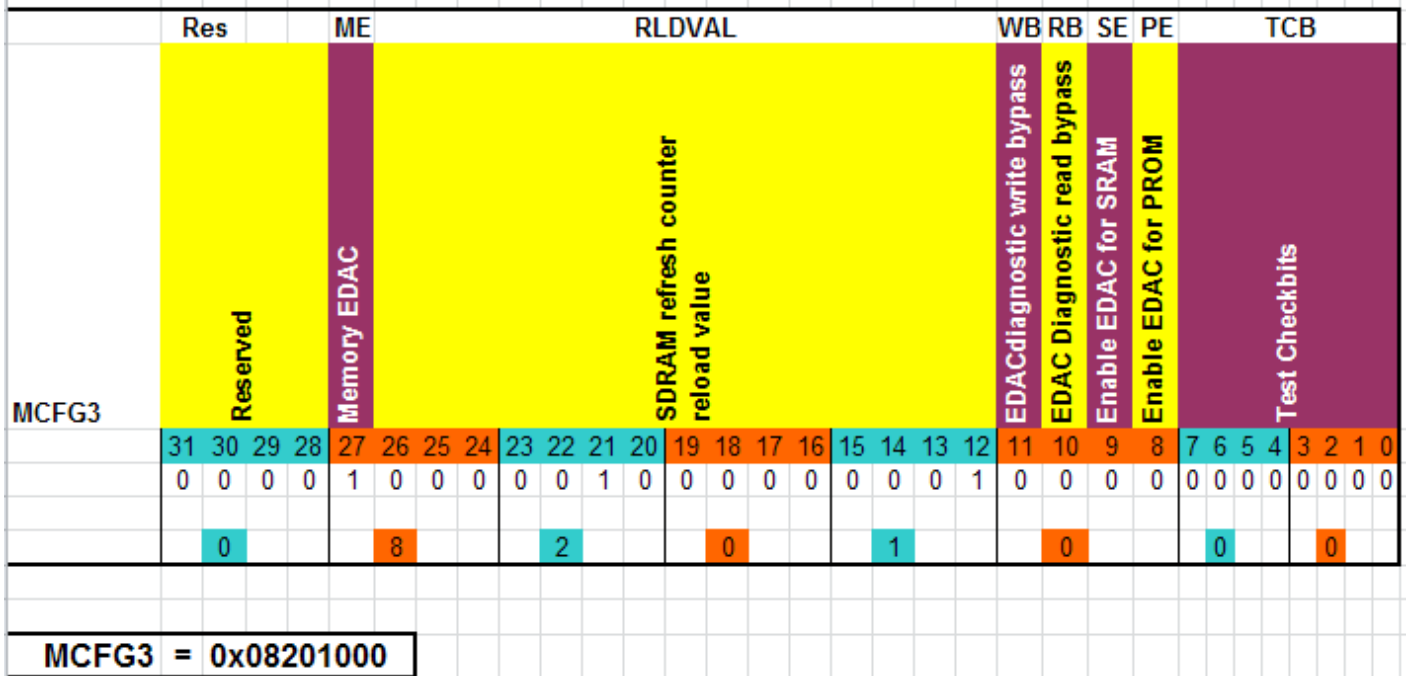


Figure 3: Memory Configuration Register 3

3.0 Conclusion

The application note and spreadsheet is intended help configure the memory configuration registers of the UT699.

4.0 References

- 4.1 Aeroflex Colorado Springs Inc., UT699 LEON 3FT/SPARCTM V8 MicroProcessor Advanced User Manual, Aug. 2010