LVDS Receiver Input Thresholds

Table 1: Cross Reference of Applicable Products

<table>
<thead>
<tr>
<th>Product Name:</th>
<th>Manufacturer Part Number</th>
<th>SMD #</th>
<th>Device Type</th>
<th>Internal PIC</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3-VOLT QUAD RECEIVER</td>
<td>UT54LVDS032LV/E</td>
<td>5962-98652</td>
<td>02, 03, 04, 05</td>
<td>WD04, WD08, WD29, WD31</td>
</tr>
<tr>
<td>3.3-VOLT QUAD RECEIVER with TERMINATION RESISTOR</td>
<td>UT54LVDS032LVT</td>
<td>5962-04201</td>
<td>01, 02</td>
<td>WD06, WD10</td>
</tr>
<tr>
<td>3.3V DUAL DRIVER and RECEIVER</td>
<td>UT54LVDM055LV</td>
<td>5962-06202</td>
<td>01</td>
<td>WD22</td>
</tr>
<tr>
<td>5.0V QUAD RECEIVER</td>
<td>UT54LVDS032</td>
<td>5962-95834</td>
<td>02</td>
<td>JR06, JR09</td>
</tr>
<tr>
<td>5.0V QUAD RECEIVER with COLD SPARE</td>
<td>UT54LVDS032</td>
<td>5962-95834</td>
<td>03</td>
<td>JR11</td>
</tr>
<tr>
<td>3.0V QUAD BUS LVDS CROSSPOINT SWITCH</td>
<td>UT54LVDM228</td>
<td>5962-01537</td>
<td>01</td>
<td>WD15, WD16</td>
</tr>
<tr>
<td>3.0V OCTAL BUS LVDS REPEATER</td>
<td>UT54LVDM328</td>
<td>5962-01536</td>
<td>01</td>
<td>WD17, WD18</td>
</tr>
<tr>
<td>3.0V DESERIALIZER with COLD SPARE</td>
<td>UT54LVDS218</td>
<td>5962-01535</td>
<td>01, 02</td>
<td>WD12, WD14</td>
</tr>
</tbody>
</table>

1.0 Overview

Low Voltage Differential Signaling (LVDS) is a method used to transmit and receive hundreds of megabits per second over differential media using a low voltage signal swing (~350mV). LVDS communications are preformed by a driver and a receiver. The LVDS receiver, see Figure 1, senses a differential voltage across the termination resistor (RT) located across the receiver input terminals (RIN+/RIN-) and outputs a standard CMOS signal (ROUT). LVDS receivers generate their output state based on the direction the current is flowing across the termination resistor.

![LVDS Receiver Diagram](image)

Figure 1. Notional LVDS Receiver diagram

Figure 2 shows the current flow through the driver/receiver system during a logic LOW state. The current flows through the termination resistor from negative to positive receiver terminals, a forward voltage drop occurs and a logical LOW appears at the output (ROUT) of the receiver. Figure 3 shows the current flow through the driver/receiver system during a logic HIGH state. Similarly, the current flows through the termination resistor from positive to negative receiver terminals, a reverse voltage drop occurs and a logical HIGH appears on the receiver output.
2.0 LVDS/LVDM Receiver Specifications

Low Voltage Differential Signaling input/output signal levels for LVDS are defined by the Telecommunications Industry Association/ Electronic Industries Association ANSI/TIA/EIA-644. ANSI/TIA/EIA-644 is an electrical standard only and does not define a protocol. Aeroflex LVDS Drivers and Receivers are compliant with this specification.

The differential input high threshold voltage, $V_{TH}$, describes the minimum positive differential voltage on the receiver inputs that results in a logic HIGH state on the receiver output (ROUT). $V_{TL}$, the differential input low threshold, describes the maximum negative differential voltage on the receiver inputs that results in a logic LOW on ROUT. Figure 4 details $V_{TH}$ and $V_{TL}$ limits with respect to ground and the maximum recommended input voltage on the receiver input pins.
LVDS receiver differential input threshold levels are guaranteed to be +/-100mV; characterization of the devices has shown voltages within these limits and can cause the receiver output to switch state. The differential input threshold sensitivities are maintained over a wide common mode from 0V to 2.4V. LVDS also features a +/-1 V common-mode range around the driver offset voltage (+1.2V typical) which aids in the rejection of system noise that is coupled between the differential pairs.

During characterization of the receivers, Aeroflex Colorado Springs has seen the MIN voltage for V\textsubscript{TH} be ~40mV, and V\textsubscript{TL} MAX be ~60mV. Results of characterization data are listed in Table 2; this data is not guaranteed.

Table 2. Typical receiver differential input threshold data

<table>
<thead>
<tr>
<th>V\textsubscript{TH} \textsuperscript{(mV)}</th>
<th>V\textsubscript{TL} \textsuperscript{(mV)}</th>
</tr>
</thead>
<tbody>
<tr>
<td>MIN</td>
<td>MAX</td>
</tr>
<tr>
<td>+40</td>
<td>+100</td>
</tr>
</tbody>
</table>

3.0 Summary

LVDS receivers are designed to reject common-mode noise. Some customers have expressed concern regarding noise immunity of the LVDS receivers due to the low voltage, +/-350mV, swing along with the +/-100mV differential receiver input thresholds. The system designer should follow good design practices and be sure the differential signals run close together through controlled impedance traces or cables. Aeroflex Colorado Springs designs LVDS receivers to ignore common mode noise that is equally coupled on the differential signals and switch only when there is a difference between the differential input signals.