Aeroflex Colorado Springs
UT8MR2M8 16M MRAM and UT8MR8M8 64M MRAM
Frequently Asked Questions

Question 1)
Why is temp range only -40 to 105C instead of full mil range?

Answer 1)
Aeroflex is currently offering a -40 to 105C temperature range at this time; however, evaluation to support full military temperature range is in progress and will be determined once full characterization is complete and yield margin analysis is understood.

Question 2)
Can MRAM be used as a replacement to EEPROMs?

Answer 2)
Yes, the Aeroflex MRAMs meets timing & density of EEPROM. It provides a simpler interface with a faster write access time.

Question 3)
Are IBIS models available for both 16 & 64M?

Answer 3)
Yes, the IBIS models are available for download from the Aeroflex website. Aeroflex takes actual product and empirically characterizes it to create IBIS models.

Question 4)
In regards to qualification strategy, have Aerospace Corporation, DLA & key customers been involved & have we received approval/comments from them?

Answer 4)
Yes, Aerospace and DLA have reviewed and approved Aeroflex's MRAM qualification approach. Aeroflex has a long history of QML qualification working with Aerospace Corporation and DLA.

Question 5)
Has Aeroflex included their usual excellent level of "new technology insertion", including collaboration with Aerospace Corporation for concurrence on Failure Mode and Effects?

Answer 5)
Yes. Aeroflex has conducted a full FMEA evaluation throughout the design, package development, assembly and test of this product. Aeroflex has coordinated this work with both DLA and the Aerospace Corporation.

Question 6)
Is an export license required for the MRAMs?

Answer 6)
Yes

Question 7)
Are the MRAM devices ITAR or only EAR99 ?

Answer 7)
The MRAM products will be ITAR controlled.

Question 8)
Is the 60 Gauss a storage or operational spec?

Answer 8)
60 Gauss is an operation specification. This is the goal for the MRAM product to operate through. The final level of magnetic immunity for the MRAM products will be specified once the final shielding can be characterized.

Question 9)
Does the MRAM include EDAC or require EDAC protection?

Answer 9)
Yes. The native 16Mb technology provides single bit error correction which is transparent to user. The 64Mb device has an MBE (multiple-bit error) flag for multi bit error detection. If a double bit is detected by the ECC during a read, the MBE flag is raised. In most instances, this is due to a SEFI during the read cycle. The user should read the address a second time. If a second MBE flag is raised, then the read address has multiple errors and the ZZ pin should be toggled to correct. An application note will be available and will provide details on proper SEFI mitigation procedures.

Question 10)
Can a single MRAM be used to replace both EEPROM for the Aeroflex LEON 3FT microprocessor and for configuration FLASH for the V5?

Answer 10)
One proposed application for the MRAM is to replace the PROM space which holds program code for the LEON. MRAMs can also be used to hold the configuration bitstream for the Virtex-5. It is not possible to use a single 64Mb MRAM for both applications simultaneously due to density and addressing requirements.

Question 11)
Have you done any integration work with the Aeroflex LEON 3FT microprocessor?

Answer 11)
Yes. The MRAM has been proposed as a replacement for the PROM space which holds the program code or kernel for the LEON 3FT

Question 12)
What size MRAM can load the boot program for the largest Xilinx FPGA?

Answer 12)
The 64Mb MCM contains the memory for a single configuration of the Virtex-5, FX130. The FX130 (SIRF, XQR5V) is the largest space qualified FPGA from Xilinx. The 64Mb MCM, or a combination of 16Mb MRAMs, can be used with the smaller XQR4V (Virtex-4) devices.

Question 13)
Is data retention 10 years?

Answer 13)
Data retention is 20 years as specified in the data sheet.

Question 14)
Do you know when the final drawing will be released for the MRAM 16 Mb device?

Answer 14)
The package outline drawings for the 40-lead dual flat-packs are finalized and in the data sheet. Two versions of the 40-lead package are shown: one with 25mil lead pitch and one with 50mil lead pitch.

Question 15)
Have you considered exposing these parts to very high magnetic fields, over 1 Tesla?

Answer 15)
The MRAM device is not designed to be exposed to very high fields greater than 1 Tesla.

Question 16)
Is development of the 64Mb MRAM + Virtex-4/5 Configurator product continuing?

Answer 16)
Yes. Aeroflex continues to work with Xilinx to evaluate the 64Mb MRAM MCM for configuration support of the Virtex-5. The Byte Peripheral Interface in the XQR5V (the Virtex-5 SIRF) supports both indirect programming of the configuration memory and power-on configuration of the XQR5V from this memory. As soon as the prototypes for the 64Mb MCM are available, Aeroflex will confirm the requirements for the MRAM to directly support the XQR5V.

Question 17)
Is there a write-protection feature to avoid any unwanted erase of code or data?

Answer 17)
The MRAM contains low-voltage inhibit circuitry to prevent data writes whenever the supply voltage drops below its minimum specified range (3.0V). The MRAM does not contain a user settable write protect mode.

Question 18)
Will the MRAM typically require compensation for systems which have a magnetic dipole requirement?

Answer 18)
The MRAM will not require compensation for systems whose magnetic dipole creates ambient magnetic fields of less than 60 Gauss.

Question 19)
Are there any expected die changes between prototype and production devices?

Answer 19)
Yes. The radiation tolerate flight MRAM product will have some enhanced and added pin functions as compared to the non-radhard prototype device. The RadTol flight MRAM will provide a true, low power sleep mode which is more comprehensive (thus lower power) than that on the prototype product. The RadTol flight MRAM will also include new pin functions which are bonded out for use with the 64Mb MRAM MCM. These include an internal decoding capability to support an enable all function (\E_all) with two additional address bits to select individual die in the 64Mb MCM. A multi-bit error flag (MBE) is also included with the RadTol flight device and bonded out in the 64Mb MCM to identify when the ECC logic has detected two bit errors during a memory read.

Question 20)
Can the EDAC be disabled for the Radiation Qualification testing? Is it going to be?

Answer 20)
Yes, the EDAC or ECC can be disabled via test modes on the 16Mb MRAM; however, it is not user accessible. Yes, Aeroflex plans to disable the ECC during heavy ion testing to determine an SEU rate for the native memory without single bit error correction.

Question 21)
How are the MRAMs programmed?

Answer 21)
Currently, the MRAMs are programmed in-system by writing address and data to the device. Aeroflex is evaluating the BP Microsystems programmer for use as a stand-alone

programming system. A specific socket module will be required for each of the MRAM package types.

Question 22)
Will post program burn-in be required?

Answer 22)
No. The MRAM memory bit is a magnetic tunnel junction, not an anti-fuse. There is no need to force current at temperature through the junction to complete a physical transformation. Rather the memory is stored by magnetically toggling the polarization in synthetic anti-ferromagnetic layers.

Question 23)
Do you expect any issues with qualification of the MCM package? Does Aeroflex have any prior experience with this type of package?

Answer 23)
Aeroflex does not anticipate any issues with the MCM package for qualification. Aeroflex has previously qualified stacked memory devices in similar planar, dual cavity MCM packages.