

UTMC Product Information Sheet

SμMMIT™ Family History and Anomalies - SJ01/SJ02 to JA01

Abstract

This document contains a brief history of the SμMMIT Family offerings, followed by design anomalies encountered and solutions administered in the more recent forms of the design's evolution. Concluding comments treat recent experiences worth highlighting such as JTAG operation in the latest SμMMIT parts.

Background

In discussing the SμMMIT Family it makes sense to refer to the particular protocol die using UTMC's four-character designator followed by a revision letter. Material covered herein includes the original SμMMIT SJ01 die, and its revisions, followed by the "enhanced" SJ02 revisions and evolution to the current JA01 die. Also contained are issues that refer to the memory management interface die (MMU), where it is applicable, including its design into the JA01 die. To help simplify the applicability of the items discussed, common package markings for product offerings can be referenced in Table 1. **Note:** The product may be purchased relative to the SMD (see table 1) or UTMC data sheet; hence, the package marked with either the UTMC part number or SMD is mutually exclusive. Further, the last column of Table 1 indicates the multi-chip module identifier and is the quickest way to see if the part contains the SJ02 or JA01 protocol die.

Table 1: SμMMIT Product Package Marking Reference

Product	SMD #	UTMC #	Protocol Die	Product PIC #
SμMMIT E	5962-92118 02	UT69151E	SJ02C	SJ02
SμMMIT E	5962-92118 03	UT69151E	JA01B	JA01
SμMMIT DXE	5962-94663 05	UT69151DXE	SJ02C	MM010
SμMMIT DXE	5962-94663 08	UT69151DXE	JA01B	MM016
SμMMIT LXE12	5962-94663 06	UT69151LXE12	SJ02C	MM012
SμMMIT LXE15	5962-94663 04	UT69151LXE15	SJ02C	MM011
SμMMIT LXE12	5962-94663 09	UT69151LXE12	JA01B	MM017
SμMMIT LXE15	5962-94663 07	UT69151LXE15	JA01B	MM018
SμMMIT XTE5	5962-94758 05	UT69151XTE5	SJ02C	MM013
SμMMIT XTE12	5962-94758 06	UT69151XTE12	SJ02C	MM014
SμMMIT XTE15	5962-94758 04	UT69151XTE15	SJ02C	MM015
SμMMIT XTE5	5962-94758 08	UT69151XTE5	JA01B	MM019
SμMMIT XTE12	5962-94758 09	UT69151XTE12	JA01B	MM020
SμMMIT XTE15	5962-94758 07	UT69151XTE15	JA01B	MM021
SμMMIT RTE	5962-98587 01	UT69151RTE	JA01B	MM022

The original SμMMIT part was built using the SJ01 die. This chip served as a 1553-bus protocol handler as a stand-alone device and in other packaging configurations. As a protocol handler, the SJ01 is programmed as a bus controller, remote terminal, or as a bus-monitoring device. Coupling the SJ01 with two transceivers in a single package, the SμMMIT was offered as the LX and DX – LX and DX differing in only transceiver supply voltage. The SJ01 was also packaged with

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memory, MMU, and two transceivers as the S μ MMIT XT. The MMU was UTMC's own UF66 memory interface die. The SJ01 had improvements such as changes to the configuration of several three-state outputs and ROM code improvements; hence, the four revisions A through D were fabricated for the SJ01. A point was reached to add several design "enhancements" and increased functionality where a simple mask revision would not suffice.

Enhancements, or new features, were introduced via micro code necessitating a new S μ MMIT die. This "enhanced" die carries the designation SJ02. Part offerings discussed in the previous paragraph remain the same, but are referred as the Enhanced S μ MMIT family, carrying the designations Enhanced S μ MMIT (stand-alone part or S μ MMIT E), LXE, DXE, and XTE. Five anomalies encountered throughout A, B, and C revisions of the SJ02, including those encountered with the MMU, were addressed during the life of the Enhanced S μ MMIT family leading to design efforts for the completely new JA01 die.

Current S μ MMIT devices use the JA01 die. This design consolidates the protocol handler (old SJ0X functionality) with the MMU and 4K X 16 worth of memory on a single die. These functional units were three separate chips in earlier SJ01 and SJ02 versions of the S μ MMIT family and Enhanced S μ MMIT family, respectively. Following is a more specific treatment of the particular issues encountered by end users and UTMC.

Design Issues

SJ02C to JA01

UTMC is actively supporting designs utilizing the latest Enhanced S μ MMIT family devices as they have superseded the original S μ MMIT parts; therefore, design issues discussed hereafter pertain to the SJ02 device revisions, the MMU, and the new JA01 devices. Several ROM changes for the SJ02 provided the need for revisions A through C, but the design wasn't manufactured until revision C. The anomalies listed below were encountered with the SJ01C, including their respective corrections, that were comprehended in the JA01.

1. An anomaly was experienced with the pending interrupt register (Register #4) not always properly clearing when read. The register clears on a read at the first occurrence, but not after subsequent interrupts. This situation was corrected in the JA01 design with changes to the ROM microcode. The pending interrupt register now clears at the occurrence of being read.
2. When a *skip* opcode follows an execute 1553 opcode resulting in a 1553 bus timeout condition, the skip time value will not function properly. Design of the JA01 addressed this and the skip time value now executes properly (a more complete treatment of the Skip Anomaly is found on UTMC's website under Data Bus Product Erratas).
3. Selecting buffer mode (burst DMA's) and circular buffer mode 02, separating data and message information, the original S μ MMIT stores the data at the data pointer plus two address locations (similar to functionality observed at election of the joined data/message option). However, the data pointer is updated with an address indicating data storage at the top of the buffer. This anomaly presents no issue for transmit commands where memory is read for transmission. This issue was not corrected in the migration to the JA01 design. Work-around documentation is available on UTMC's website under Data Bus Product Information Sheets.
4. Upon enabling *ping pong* mode, the register bit indicating acknowledgment of *ping pong* mode is not updated until a 1553 command is received. Despite the case where the part starts up in ping pong mode, acknowledgement of *ping pong* mode is not readily indicated either. Designing the JA01 addressed this issue. Devices using the new JA01 no longer exhibit the misbehavior.
5. The last issue for the SJ02 was that several outputs were not being properly reset at assertion of an asynchronous reset. By changing the buffer types in the JA01 design this anomaly was corrected.

In addition to the changes made concerning the SJ02 there were two items addressed in the MMU functionality as this circuitry was designed into the JA01.

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Original MMU Die Incorporated into the JA01

There were two issues addressed on the MMU memory interface that were incorporated in designing the JA01. The first anomaly requires the ALE signal function to be surrounded by positive clock edges when the part is in 8-bit multiplexed mode. The second anomaly occurs in 8-bit non-multiplexed mode. This MMU issue requires stability of all address lines through both writes (MMU requires writing in pairs) except for the least significant address bit (A[0]). Address bit 0 must toggle to indicate to the MMU whether the data word is an upper or lower byte.

Design issues encountered in the MMU were dealt with by incorporating the memory interface into the single JA01 die thus consolidating the MMU and the protocol handler. The ALE now performs as documented in the original specification. ALE now controls the latching of the correct address upon its low assertion (in multiplexed mode). The second MMU issue solved in the JA01 design was the requirement for the address bus to remain stable during two writes. One write is required during the originally specified hold time.

Issues Necessitating B Revision of JA01

Fabricating the first revision of the JA01, incorporated the MMU and the protocol handler into a single die, resulting in several new design anomalies. Listed below are the issues encountered including their corrections where appropriate.

1. Self-test caused an internal memory corruption. When self-test was triggered by a register write there seems to be no issue. However, when the self test is initiated over the 1553 bus, the memory was evidently corrupted. This issue was corrected in the JA01B. A correct and complete self test is performed through both the registers and over the 1553 bus.
2. The JA01 introduced an issue occurring during autoenable. The part will not check the mode of operation from the operational status register (Register 1), but instead relies upon the mode read from memory during autoenable. This issue is not corrected.
3. In the A revision JA01 the Auto-Initialization byte order was discovered to be reversed in comparison to the original functionality. This situation is rectified in the second spin of the JA01 (revision B).
4. It was discovered that in the case where a host makes a memory access while the S μ MMIT is also doing so, $\overline{\text{RDY}}$ was asserted by the S μ MMIT before the host access had been completed. This showed the memory location as being corrupt (i.e. a read of the wrong data or an incorrect write by the host). $\overline{\text{RDY}}$ is now held high until both the host and the S μ MMIT have completed their respective memory accesses.

New JTAG functionality in the JA01 S μ MMIT Family

In the process of converging the memory management interface and the protocol handling circuitry into a single die (JA01), two separate JTAG boundary scan registers have also become a single unit. Although the two separate boundary scan registers is applicable to the XTE and RTE offerings, all the JA01 devices have a different BSR from the SJ02 devices. Further, the former input, output, and mode select pins for the memory management interface were eliminated in the JA01 XTE and RTE S μ MMIT JTAG. **The former TDIM and TMSM must be tied to V $_{\text{SS}}$ on the JA01 version of the XTE** while the former TDOM is a no connect pin. Boundary scan register length, instructions, and user code have also changed in the new JA01 JTAG. A full treatment is given in a separate UTMC Application Note.