

UT200SpW16RTR-EVB 16-Port SpaceWire Router Evaluation Board

User Manual

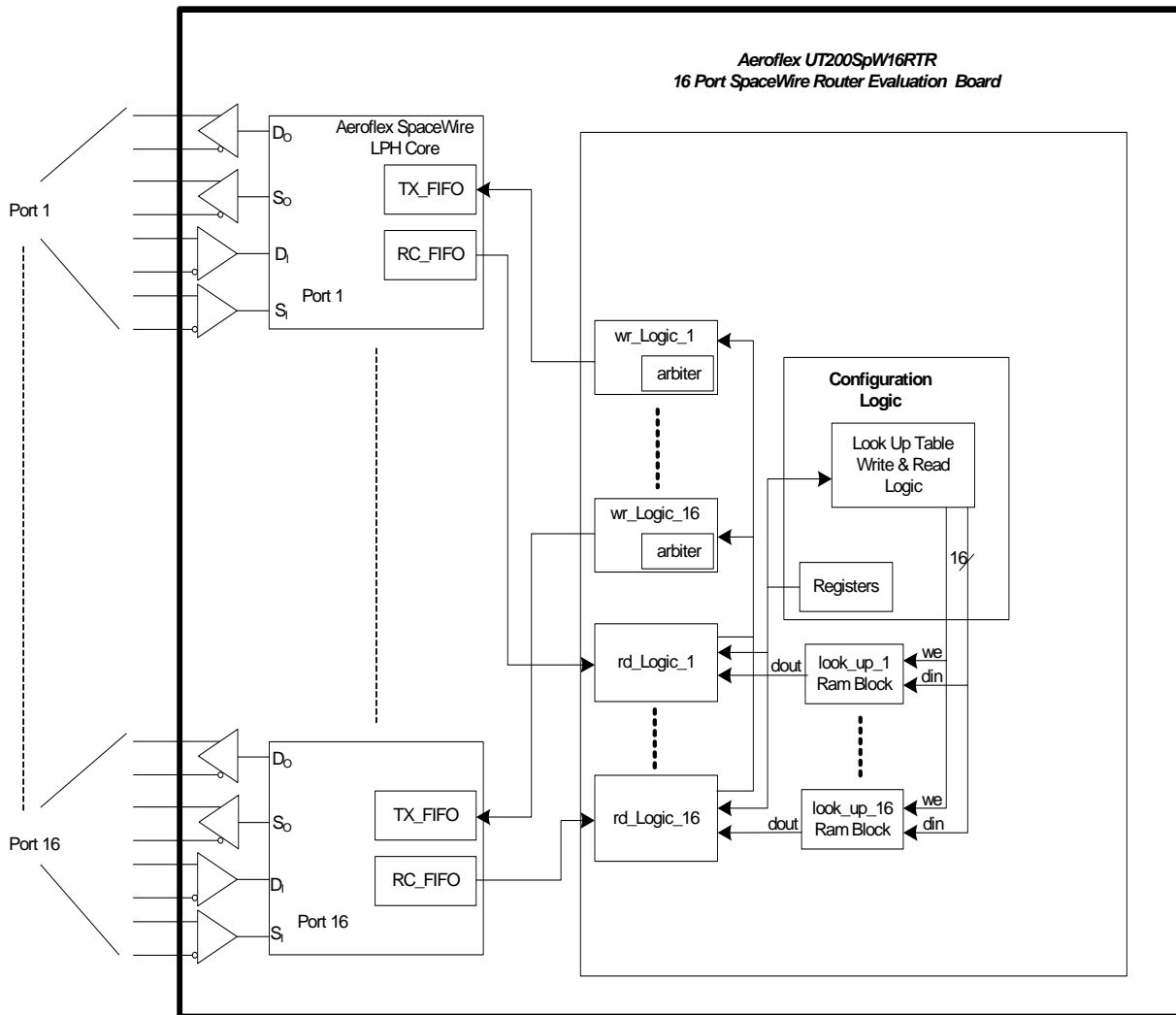
December 17, 2008

www.aeroflex.com/SpaceWire



INTRODUCTION

The UT200SpW16RTR-EVB is a 16-Port SpaceWire Router evaluation board which is designed to provide all 16-receive ports access to all 16-transmit ports. This is achieved by using a “round robin” arbitration scheme which gives each of the 16-receive ports equal access to each of the 16-transmit ports. Path and Logical Addressing are supported as defined in the SpaceWire Standard (document number ECSS-E-50-12A). A copy of the standard can be downloaded at <http://www.ecss.nl/>. Each port has a dedicated block of memory for lookup table data and serves to prevent each port from having to arbitrate for a shared memory space lookup table. A higher level protocol is used to configure the router, as well as to read status and send a number router commands. Configuration may be performed through any one of the 16 ports. The status registers provided allow the user to monitor the network using the configuration protocol. A “group adaptive” function for two ports is also included and allows an alternate transmit path for received data in the event the primary transmit path is busy.



UT200SpW16RTR SpaceWire Router Evaluation Board

1. SCOPE

This document describes the features and necessary steps to set-up and operate the Aeroflex SpaceWire 16-port Router Evaluation Board.

2. REFERENCE DOCUMENT

The SpaceWire Standard, ECSS-E-50-A can be downloaded at <http://www.escc.nl/>.

3. FUNCTIONAL DIAGRAM

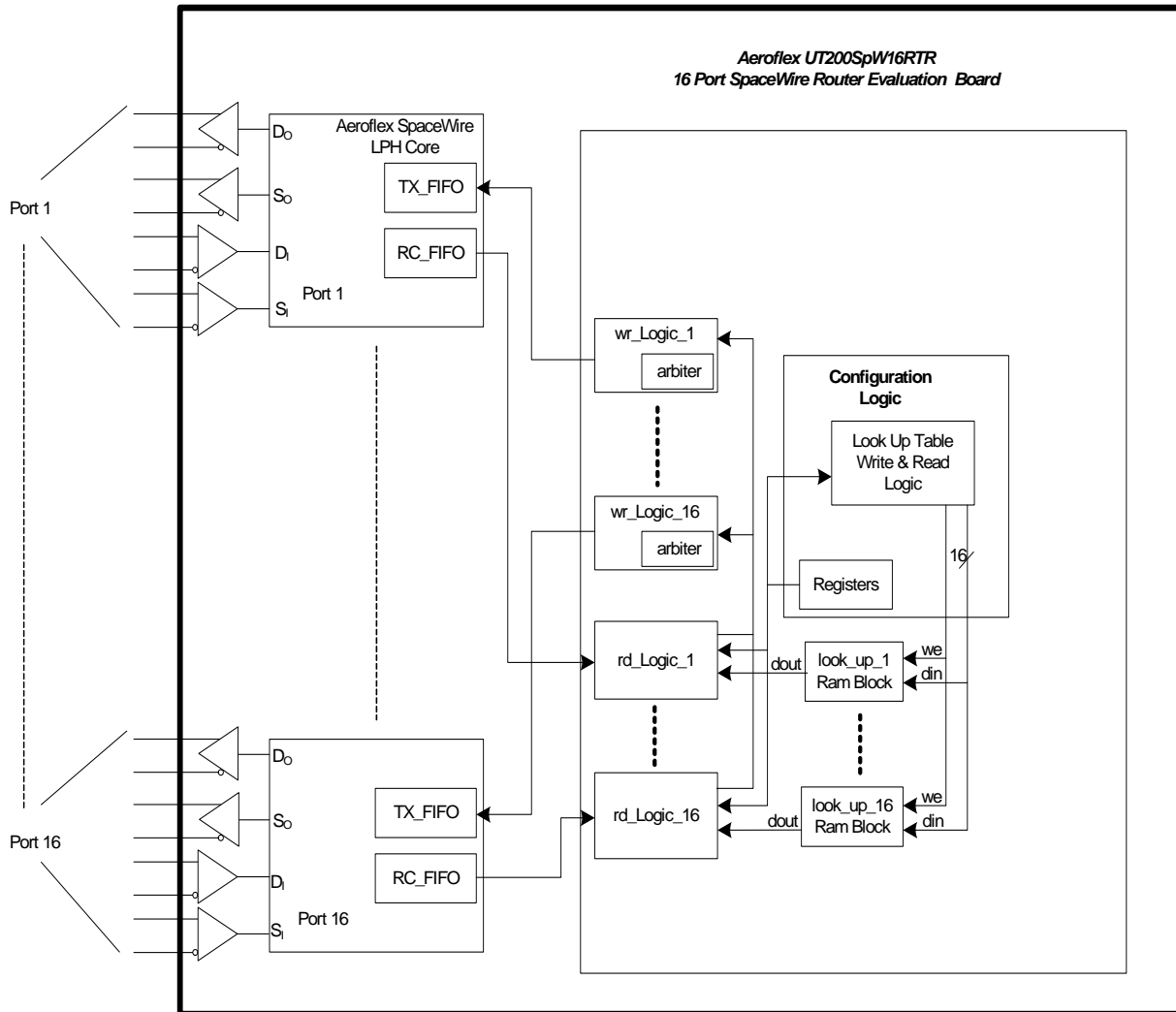


Figure 1. Functional Block Diagram

4. FEATURES AND GENERAL OPERATION

4.1 Features

The Aeroflex 16-Port SpaceWire Router is designed to provide all 16 of the receive ports access to all 16 of the transmit ports. This is achieved by implementing a “round robin” arbiter in each of the transmit write logic blocks. The arbiter activates whenever any of the 16 read logic blocks requests access to a write logic block. The arbiters in each of the 16 write logic blocks counts from 1 to 16 with the result being if two ports request the bus at exactly the same time, the lowest number port requested gets access first. In addition, the router provides the following features.

1. Path Addressing
2. Logical Addressing
3. Group Adaptive Routing (2 ports only)
4. Configuration access through any one of the 16 ports
5. Identical lookup tables for each port so no arbitration is required

4.2 Development Board Set-Up

When the router is first powered up all ports will be enabled by default. To disable a port refer to Section 5 on configuration of the router. If only path addressing is required, no configuration transactions are required. If logical addressing is required, then the lookup tables need to be loaded with the desired data. This is performed following the configuration protocol specified in section 5. Before sending time codes, the user must first set the router port that is connected to the “time master” node. Refer to sections 8.13 and 10 for more information on time codes.

4.2.1 Power Requirements

The Aeroflex SpaceWire Evaluation Board can be powered either by plugging the card into a 6U CPCI slot or by applying 3.3 V and 5V to the BNC connectors on the board.

4.2.2 Front Panel

The front panel has the ON/OFF switch, 4 LED’s, the 3.3V current monitor SMA connector and the 16 SpaceWire connectors.

4.2.2.1 Power Switch

The toggle switch on the front panel is used to turn on the router board. The up position is “ON” and the down position is “OFF”.

4.2.2.2 Front Panel Led

Currently only the top LED is used by the Evaluation Board. This LED is used to indicate when the router has loaded the bit file stored on the on-board PROM.

4.2.2.3 SpaceWire16-Port Connectors

The SpaceWire Standard defines the SpaceWire connector is a 9 pin micro-mini D type. Pin assignments for each of the router connectors are defined in Figure 2.

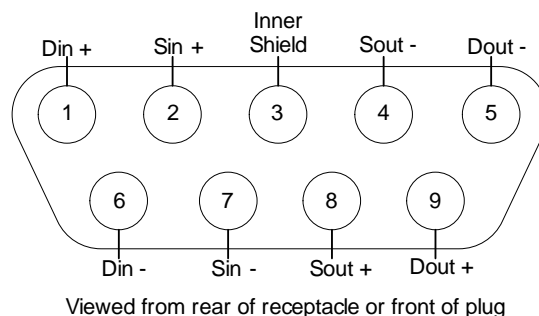


Figure 2. SpaceWire Connector Pin Definitions

4.2.3 Setting Transmit Speed

The router currently has 4 settings for transmit speeds on all ports. The choices are 120Mbps, 100Mbps, 80Mbps and 40Mbps. These transmit rates are controlled by the SW2 switch.

4.2.3.1 SW2

Switch 2 has the Clock Select signals connected to it. Figure 2 shows the connections to SW2 while Table shows the frequency associated with each setting.

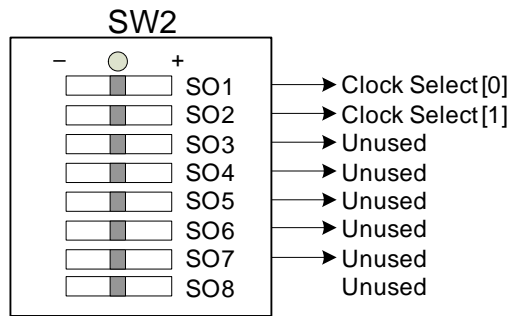


Figure 3. SW2 Connections

4.2.3.2 SW2 Settings

SW2 controls the operating frequency of the router. There are four frequencies that can be set and these are defined in Table 1. All ports on the router operate at the data rate specified by SW2.

Table 1. SW2 Settings	
SW2 Setting	Frequency
00	120Mbps
01	100Mbps
10	80Mbps
11	40Mbps

4.2.4 FIFO Clock

The clock used to read and write to all of the FIFOs. The FIFO clock is fixed at 50MHz.

4.3 Sending Packets

The first byte of data received on the SpaceWire bus after power up or after an EOP/EEP (these are treated the same by the router) will be the header byte. The header byte determines whether path addressing (0x01 to 0x1F), logical addressing (0x20 to 0xFF), or a configuration transaction 0x00 occurs. If there has been no configuration write transaction, then only path addressing will be supported since the lookup tables have not been configured. Currently, there are no restrictions on the size of the packets that can be sent through the router.

4.3.1 Bad Packet

Packets that do not have a valid "path address" or a logical address that has not been configured will be considered bad packets. Bad packets will be read from the receive FIFO, but not sent to any of the transmit FIFOs. This is commonly known as "Spilling the Packet".

5.0 CONFIGURATION PROTOCOL

The Aeroflex SpaceWire Router is configured through any one of the 16 SpaceWire ports. The first byte of data with a value of 0X00 received by any router port after reset or an EOP/EEP initiates a configuration transaction. Configuration transactions allow access to the lookup tables, configuration registers and status registers. The packet protocols for configuration reads and writes are specified in the following two sections.

5.1 Configuration Write

The write packet writes a 16-bit data word to the specified 16-bit address location in the configuration memory space. The packet begins with zero or more hardware or logical address bytes followed by the final destination address byte set to zero. Next, the router ID byte should be set to the value in the router ID register. The packet type byte should be set to write, followed by the address least significant byte, the address most significant byte, the data least significant byte and the data most significant byte. The last byte will be the arithmetic checksum value, which is an arithmetic sum of the final destination address, the router ID, the packet type, the address and data bytes. If the checksum value does not match, the command will not be executed. If the packet has less than eight (8) bytes or the checksum value is not the last byte, the command will not be executed.

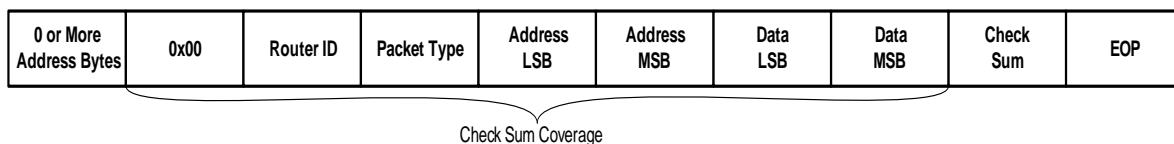


Figure 4. Configuration Port Write Packet Command

5.2 Configuration Read

The read packet will read a number (Count) of 16-bit data values from consecutive 16-bit address locations and transmit the data to the return location specified. This packet begins with zero or more hardware or logical address bytes followed by the final destination address byte set to zero. Next, the router ID byte should be set to the value in the router ID register, unless the router ID is being read. The packet type byte should be set to read, followed by the address least significant byte, the address most significant byte, the word count byte, and one or more return path address byte(s). The order of the return path address bytes are to read in the order they are received, i.e., the first return path address byte will be the path out of the first router with subsequent bytes to be used for the next layers of routers. The last byte will be the checksum value, which is an arithmetic sum of the destination address, router ID, packet type, address bytes, data bytes and return path bytes. If the checksum received does not match the calculated value, an error at the end of packet will be sent to the return address. The word count byte must be greater than zero. A value of zero causes the command to not be executed. The return address path must contain one or more bytes and the first header byte must not be zero; otherwise the command will be considered invalid and not be executed. Figure 5 shows the bytes required for a read packet command.

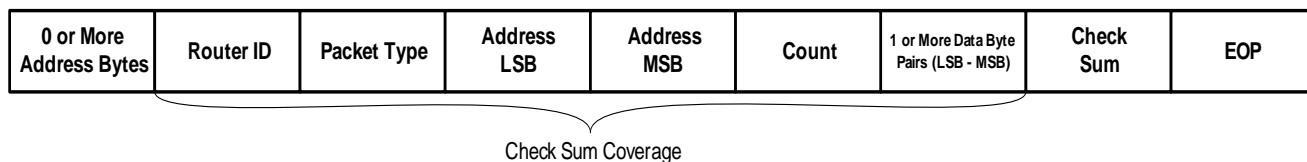


Figure 5. Configuration Port Read Packet Command

5.3 Configuration Read Response

The read response will follow the protocol shown in Figure 6.

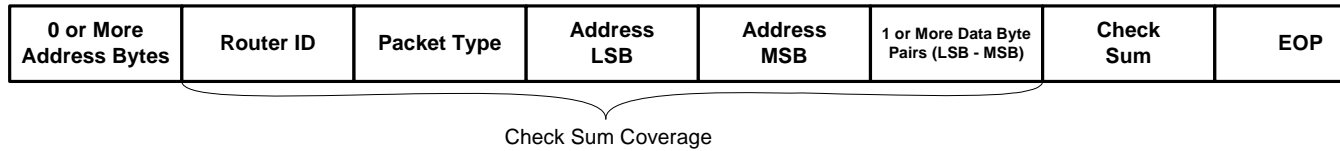


Figure 6. Configuration Port Read Packet Response

5.4 Packet Type Byte Definition

The various configuration protocols define a “packet type” byte. This byte tells the router or the user in the case of the read response type what type of transaction is being commanded or received. Table 2 defines the different packet types.

Table 2. Packet Type Definitions	
Packet Type	Value (Hex)
Write	0x00
Read No Clear	0x01
Read Clear	0x02
Read Response	0x03
Reserved	0x04-0xFF

5.5 Configuration and Status Registers

The router has a number of configuration and status registers which are used for initial setup of the router and for monitoring the router’s performance. Table 3 is a summary of all the router registers with detailed descriptions outlined in each subsection.

5.5.1 Router Identification Register

The router identification register is accessed through configuration address 0x0100. The router ID defaults to 0x00 upon reset and the user can write an 8-bit value using the configuration write protocol and using 00 for the router ID byte in the protocol.

5.5.2 Receive FIFO Reset

Writing to address 0109 and setting any or all of the 16 bits resets the appropriate Receive FIFO. For example, setting bit 0 will reset Port 1 Receive FIFO. Setting bit 1 will reset Port 2 Receive FIFO and so on.

5.5.3 Transmit FIFO Reset

This 16-bit register at address 0x010F is used to reset any or all of the transmit FIFOs. Bit 0 will reset Port 1, Bit 1 will reset Port 2 and so on.

5.5.4 Version Register

This read only register located at address 0x0101 tells the user what version of the Aeroflex Router is contained within the on-board PROM.

Table 3. Configuration Summary Table

R/W	ADDRESS (HEX)	NAME	DEFAULT (HEX)	DESCRIPTION
R/W	0020-00FF	Lookup Table	0000	Logical address lookup table
R/W	0x0100	Router ID	0000	Router identification register
R	0x0101	Version Register	N/A	Router version register
W	0x0109	Receive FIFO Reset	N/A	Used to reset any or all of the receive FIFOs
W	0x010F	Transmit FIFO Reset		Used to reset any or all of the transmit FIFOs
R/W	0x010A	Configure Port Enable	FFFF	Using this register, ports can be enabled or disabled as configuration ports
R	0x010D	Link Run Register	N/A	Indicates which ports are in the run state. One bit for each port
R	0x010E	Transmit Full Register	N/A	Transmit FIFO full register. Indicates which transmit FIFO's are full, one bit for each transmit FIFO
W	0x0110	Router Reset	N/A	A write command to this address will reset the entire router. The data in this is....
R	0x0111-0x0114	Router Error Count	N/A	Router error count registers. Each nibble within these registers represents the error count for a given router port.
R/W	0x0116	Link Disable Register	0000	Enables or disables individual links
R/W	0x0117	Autostart	0000	One bit per port enables autostart for that port
R	0x0118 to 0x0128	Port Busy Registers	N/A	These registers indicate the current receive port to transmit port connection. Address 0118 is for receive port 1 and address 0127 is for receive port 16.
R/W	0x0128	Time Master Select	0000	This register is used to select which port on the router is connected to the note that is the system time manager.

5.5.5 Configurable Port Enable

At power up all of the ports on the router can be used to configure the router. This read and write register at address 0x010A allows the user the ability to specify which ports can be used as configuration ports. Refer to Table 4 below for the bit mapping for this register.

Table 4. Configure Port Enable

ADDRESS (HEX)	BIT NUMBER	DESCRIPTION AND COMMENTS	
		Low	High
0x010A	0	Disable Port 1	Enable Port 1
	1	Disable Port 2	Enable Port 2
	2	Disable Port 3	Enable Port 3
	3	Disable Port 4	Enable Port 4
	4	Disable Port 5	Enable Port 5
	5	Disable Port 6	Enable Port 6
	6	Disable Port 7	Enable Port 7
	7	Disable Port 8	Enable Port 8
	8	Disable Port 9	Enable Port 9
	9	Disable Port 10	Enable Port 10
	10	Disable Port 11	Enable Port 11
	11	Disable Port 12	Enable Port 12
	12	Disable Port 13	Enable Port 13
	13	Disable Port 14	Enable Port 14
	14	Disable Port 15	Enable Port 15
	15	Disable Port 16	Enable Port 16

5.5.6 Link Run Register

This 16-bit register at address 0x010D indicates to the user which ports are in the run state. Bit 0 is for port 1 and bit 15 is for Port 16.

5.5.7 Transmit Full Register

This 16-bit register at address 0x010E indicates to the user which Transmit port FIFO's are full. Bit 0 is for port 1 and bit 15 is for Port 16.

5.5.8 Router Reset

A write command to the address 0x0110 resets the entire router portion of the V4. SpaceWire ports are not reset, only the router that includes the state machines used to select ports and read and write to FIFO's. It is important to note, however, that the router ID at address 0x0100 will reset when a router reset command has been issued.

5.5.9 Router Error Count

There are four 16-bit registers on the router to manage error counting. Each register contains the output of a four 4-bit counter. Refer to Table 5 below for addresses of the router error counters.

Table 5. Router Error Count Register

ADDRESS (HEX)	RANGE	ERROR COUNTER
0x0111	[3:0]	Port 1
	[7:4]	Port 2
	[11:8]	Port 3
	[15:12]	Port 4
0x0112	[3:0]	Port 5
	[7:4]	Port 6
	[11:8]	Port 7
	[15:12]	Port 8
0x0113	[3:0]	Port 9
	[7:4]	Port 10
	[11:8]	Port 11
	[15:12]	Port 12
0x0114	[3:0]	Port 13
	[7:4]	Port 14
	[11:8]	Port 15
	[15:12]	Port 16

5.5.10 Link Disable Register

All ports on the SpaceWire Router can be enabled or disabled by performing a configuration write command into register 0x0116. The ports can be enabled or disabled by setting bits in the link disable register. Table 6 shows the mapping of the link disable register to the correct ports.

5.5.11 Parity Error Registers

The parity error register located at address 0x0115 (not to be confused with SpaceWire parity error) is used to indicate to the user when a lookup table access has generated a parity error. Refer to section 6.2.15 for a definition of the parity bit in the lookup table data. Bit 5 of the registers indicates there has been a parity error during a lookup table access. Bits 4 to 0 shows the last receive port transaction that the parity error occurred.

5.5.12 Autostart Registers

The autostart requirement specified in the SpaceWire Standard is implemented as a 16-bit register in the router device. The user performs a configuration write command at address 0x0117 to set any of the 16 bits to select which ports have autostart enabled. For reference Port 1 is enabled with bit 0 and Port 16 is enabled with bit 15. The autostart function is designed cause the initialization state machine within each router port to transition from the ready to the started state when a null character is received. **Note:** if the nodes connected to the router also have autostart enabled, then the link will never transition to the started state. This is because nulls are not sent by the node until the initialization state machine transitions to the started state.

Table 6. Link Disable Register

ADDRESS (HEX)	BIT NUMBER	DESCRIPTION AND COMMENTS	
		High	Low
0x0116	0	Disable Port 1	Enable Port 1
	1	Disable Port 2	Enable Port 2
	2	Disable Port 3	Enable Port 3
	3	Disable Port 4	Enable Port 4
	4	Disable Port 5	Enable Port 5
	5	Disable Port 6	Enable Port 6
	6	Disable Port 7	Enable Port 7
	7	Disable Port 8	Enable Port 8
	8	Disable Port 9	Enable Port 9
	9	Disable Port 10	Enable Port 10
	10	Disable Port 11	Enable Port 11
	11	Disable Port 12	Enable Port 12
	12	Disable Port 13	Enable Port 13
	13	Disable Port 14	Enable Port 14
	14	Disable Port 15	Enable Port 15
	15	Disable Port 16	Enable Port 16

6.0 PORT ADDRESSING

6.1 Path Addressing

For any byte received immediately after an EOP/EEP byte with the value 0x01 to 0x10 in Hex, path addressing will be implemented. Since the Aeroflex router has 16 ports, only addresses from 0x01 to 0x10 are supported. Addresses from 8'h11 to 8'h1F will be ignored. The entire port address space is defined in Table 7.

Table 7. Header Byte Memory Map

PORT ADDRESS BYTE (HEX)	PORT
0x00	Configuration access
0x01	Path Address for Port 1
0x02	Path Address for Port 2
0x03	Path Address for Port 3
0x04	Path Address for Port 4
0x05	Path Address for Port 5
0x06	Path Address for Port 6
0x07	Path Address for Port 7
0x08	Path Address for Port 8
0x09	Path Address for Port 9
0x0A	Path Address for Port 10
0x0B	Path Address for Port 10
0x0C	Path Address for Port 12
0x0D	Path Address for Port 13
0x0E	Path Address for Port 14
0x0F	Path Address for Port 15
0x10	Path Address for Port 16
0x11 to 0x1F	Not Used
0x20 to 0xFF	Logical address locations

6.2 Logical Addressing

There are 16 lookup tables (one for each port) on the router. Each lookup table is 224 by 16 and all 16 lookup tables have the same data written into them using the Configuration Protocol described in Section 5. The format for the lookup table data is described in the following sections.

6.2.1 Lookup Table Data Format

The lookup tables on the router are organized into 16 bits and are organized as shown in Table 8.

Table 8. Lookup Table Data Format

Parity	Unused			Enable Group Adaptive	Enable Header Delete	Group Adaptive Address Bits					Primary Logical Address Bits				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

6.2.11 Primary Logical Address Bits

The five LSB bits [4:0] are the primary logical address bits and are for selecting ports 1 through 16 regardless of whether group adaptive has been enabled or not. When group adaptive has been enabled, the router looks at the port address specified by these bits first and if that port is busy, then looks at the port specified by the group adaptive address bits.

6.2.12 Group Adaptive Address Bits

Bits [9:5] are used when group adaptive has been enabled and the port selected by the primary logical address bits is busy.

6.2.13 Enable Header Delete Bit

Bit [10] is used to enable the header delete function for the port selected by either the group adaptive address bits or the primary logical address bits. Whenever this bit is set high the Router deletes the header before sending the packet out of the requested transmit port.

6.2.14 Enable Group Adaptive Bit

Bit [11] is used to enable the group adaptive function on the router. Setting this bit high tells the Router to use bits [9:5] for the port select in the event the port select for the primary address bits is busy.

6.2.15 Parity Bit

A parity bit is included for each lookup table location. The parity is odd. When the header byte is decoded and falls between address 0x20 and 0xFF, a lookup table address will be retrieved by the lookup table. The parity will be calculated based on the bits in the lookup table not including the parity bit. The parity then compares the calculated parity and if they are not the same, the packet will be read out of the receive FIFO, up to and including, the EOP. This is commonly referred to as "Spilling the Packet". Additionally, the parity error register will be incremented.

7.0 ROUTER ARCHITECTURE

The following subsections and descriptions provides the user with some necessary information to interface on the Aeroflex Router.

7.1 Transmit and Receive FIFOs

Each of the 16 SpaceWire ports has a transmit and a receive FIFO that are 9-bits wide by 512 deep. The EOP and EEP handling are as specified in the SpaceWire Standard when using a 9-bit FIFO and is as follows.

Table 9. EOP and EEP Handling

9-BIT DATA	CHARACTER TYPE
100000000	EOP
100000001	EEP

7.2 Read and Write FIFO Logic

The logic implemented to read from the receive FIFO and write to the transmit FIFO is such that the router will be able to maintain the maximum data rate set by SW2 which is 120Mbs.

7.3 Arbitration

Each transmit FIFO write logic block contains an arbiter that manages the flow of data from each of the 16 receive ports to the individual transmit port. The arbiter is a “round robin” type and gives each receive port equal opportunity for access. The arbiter starts counting whenever a request for that port is received from any of the 16 receive ports. The count is from Port 1, Port 2, etc. until the count reaches Port 16 and then starts over. If a transmit port receives a request for example from Port 1 and Port 5 at the same time, the Port 1 packet will be sent first. In addition, if during the time that the Port 1 packet gets sent a packet from Port 3, the Port 3 packet will be sent before Port 5 because of the way the arbiter counts.

8.0 TIME CODES

Time codes are handled as described in the SpaceWire standard. Any valid time code received on a router port will be sent to all of the other ports of the router. A valid time code is defined as a time code value that is one greater than the previous time code value.

9.0 JUMPER SETTINGS

Currently the two 50 pin headers labeled J8 and J9 are unused. All other jumper's should be set as shown below in Table 11.

Table 10. Jumper Settings

JUMPER NUMBER	NAME	SETTING
J1	cPCI Connector	
J2	HSWAP	Leave Open
J3	V-4	Leave Open
J4	PROM	Leave Open
J5	V4 Mode	Jumper to GND
J6	V4 Mode	Jumper to GND
J7	V4 Mode	Jumper to GND
J8	LVDSP	Unused
J9	LVDSP	Unused
J10	1.8V PROB	Jumpered
J11	RCV OSC EN	Open
J12	3.3V BNC	Apply 3.3V if not using cPCI
J13	Current Monitor SMA connector	Connect DMM for power monitor of V4 3.3 supply
J14	PROB	Leave Open
J15	5V BNC	Apply 5V if not using cPCI

10.0 LVDS ELECTRICAL CHARACTERISTICS

The on-board FPOGA has on-chip LVDS buffers with integrated 100 termination for LVDS receivers. The characteristics for the LVDS buffers are shown in the following two subsections. The speed grade for the FPGA on the Aeroflex Router Development Board is 11.

10.1 DC Characteristics

Table 12 contains the DC characteristics of the LVDS buffers on the on-board FPGA device family.

Table 11. On-Board FPGA LVDS DC Characteristics

LVDS DC Specifications (LVDS_25)						
Table 9: LVDS DC Specifications						
Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CC0}	Supply Voltage		2.38	2.5	2.63	V
V_{OH}	Output High Voltage for Q and \bar{Q}	$R_T = 100\Omega$ across Q and \bar{Q} signals			1.602	V
V_{OL}	Output Low Voltage for Q and \bar{Q}	$R_T = 100\Omega$ across Q and \bar{Q} signals	0.898			V
V_{ODIFF}	Differential Output Voltage ^(1,2) (Q – \bar{Q}), Q = High (\bar{Q} – Q), \bar{Q} = High	$R_T = 100\Omega$ across Q and \bar{Q} signals	247	350	454	mV
V_{OCM}	Output Common-Mode Voltage	$R_T = 100\Omega$ across Q and \bar{Q} signals	1.125	1.250	1.375	V
V_{IDIFF}	Differential Input Voltage (Q – \bar{Q}), Q = High (\bar{Q} – Q), \bar{Q} = High		100	350	600	mV
V_{ICM}	Input Common-Mode Voltage		0.3	1.2	2.2	V

Notes:
1. Recommended input maximum voltage not to exceed $V_{CC0} + 0.2V$.
2. Recommended input minimum voltage not to go below $-0.5V$.

10.1 DC Characteristics

The switching characteristics of the on-board LVDS buffers are shown in Table 12.

Table 12. On-Board FPGA LVDS AC Characteristics

Parameter	Description	Value	Units
T_{IOPI}	Delay from I/O pad to input of the LVDS buffer	1.15	ns
T_{IOOP}	Delay from the output of the LVDS buffer to the I/O pad on the device	1.71	ns
T_{IOTP}		1.71	ns

11.0 ON-BOARD FPGA PIN LIST AND DESCRIPTION

SIGNAL NAME	PIN NUMBER	DESCRIPTION
RXAdatap1	AJ22	Port 1 Transmit Data LVDS Positive
RXAdatan1	AJ21	Port 1 Transmit Data LVDS Negative
RXAstrobep1	AC15	Port 1 Transmit Strobe LVDS Positive
RXAstroben1	AB15	Port 1 Transmit Strobe LVDS Negative
TXAdatap1	AB22	Port 1 Receive Data LVDS Positive
TXAdatan1	AH22	Port 1 Receive Data LVDS Negative
TXAstrobep1	AL14	Port 1 Receive Strobe LVDS Positive
TXAstroben1	AK14	Port 1 Receive Strobe LVDS Negative
RXAdatap2	AG21	Port 2 Transmit Data LVDS Positive
RXAdatan2	AF20	Port 2 Transmit Data LVDS Negative
RXAstrobep2	AF14	Port 2 Transmit Strobe LVDS Positive
RXAstroben2	AF13	Port 2 Transmit Strobe LVDS Negative
TXAdatap2	AE21	Port 2 Receive Data LVDS Positive
TXAdatan2	AF21	Port 2 Receive Data LVDS Negative
TXAstrobep2	AP15	Port 2 Receive Strobe LVDS Positive
TXAstroben2	AN15	Port 2 Receive Strobe LVDS Negative
RXAdatap3	AC19	Port 3 Transmit Data LVDS Positive
RXAdatan3	AC18	Port 3 Transmit Data LVDS Negative
RXAstrobep3	AD16	Port 3 Transmit Strobe LVDS Positive
RXAstroben3	AF15	Port 3 Transmit Strobe LVDS Negative
TXAdatap3	AN20	Port 3 Receive Data LVDS Positive
TXAdatan3	AP20	Port 3 Receive Data LVDS Negative
TXAstrobep3	AD17	Port 3 Receive Strobe LVDS Positive
TXAstroben3	AC17	Port 3 Receive Strobe LVDS Negative
RXAdatap4	AM20	Port 4 Transmit Data LVDS Positive
RXAdatan4	AL19	Port 4 Transmit Data LVDS Negative
RXAstrobep4	AB17	Port 4 Transmit Strobe LVDS Positive
RXAstroben4	AB16	Port 4 Transmit Strobe LVDS Negative
TXAdatap4	AL18	Port 4 Receive Data LVDS Positive
TXAdatan4	AM18	Port 4 Receive Data LVDS Negative
TXAstrobep4	AM17	Port 4 Receive Strobe LVDS Positive
TXAstroben4	AM16	Port 4 Receive Strobe LVDS Negative
RXAdatap5	B23	Port 5 Transmit Data LVDS Positive
RXAdatan5	A23	Port 5 Transmit Data LVDS Negative
RXAstrobep5	A26	Port 5 Transmit Strobe LVDS Positive
RXAstroben5	B26	Port 5 Transmit Strobe LVDS Negative
TXAdatap5	A24	Port 5 Receive Data LVDS Positive
TXAdatan5	A25	Port 5 Receive Data LVDS Negative
TXAstrobep5	G15	Port 5 Receive Strobe LVDS Positive
TXAstroben5	H25	Port 5 Receive Strobe LVDS Negative
RXAdatap6	C23	Port 6 Transmit Data LVDS Positive
RXAdatan6	C24	Port 6 Transmit Data LVDS Negative
RXAstrobep6	F25	Port 6 Transmit Strobe LVDS Positive
RXAstroben6	F26	Port 6 Transmit Strobe LVDS Negative
TXAdatap6	D24	Port 6 Receive Data LVDS Positive
TXAdatan6	D25	Port 6 Receive Data LVDS Negative
TXAstrobep6	B27	Port 6 Receive Strobe LVDS Positive
TXAstroben6	C27	Port 6 Receive Strobe LVDS Negative
RXAdatap7	F23	Port 7 Transmit Data LVDS Positive
RXAdatan7	E23	Port 7 Transmit Data LVDS Negative
RXAstrobep7	D26	Port 7 Transmit Strobe LVDS Positive
RXAstroben7	F26	Port 7 Transmit Strobe LVDS Negative

TXAdatap7	D24	Port 7 Receive Data LVDS Positive
TXAdatan7	D25	Port 7 Receive Data LVDS Negative
TXAstrobep7	B27	Port 7 Receive Strobe LVDS Positive
TXAstroben7	C27	Port 7 Receive Strobe LVDS Negative
RXAdatap8	G23	Port 8 Transmit Data LVDS Positive
RXAdatan8	H24	Port 8 Transmit Data LVDS Negative
RXAstrobep8	A28	Port 8 Transmit Strobe LVDS Positive
RXAstroben8	A29	Port 8 Transmit Strobe LVDS Negative
TXAdatap8	B25	Port 8 Receive Data LVDS Positive
TXAdatan8	C25	Port 8 Receive Data LVDS Negative
TXAstrobep8	J25	Port 8 Receive Strobe LVDS Positive
TXAstroben8	K26	Port 8 Receive Strobe LVDS Negative
RXAdatap9	D12	Port 9 Transmit Data LVDS Positive
RXAdatan9	C12	Port 9 Transmit Data LVDS Negative
RXAstrobep9	B10	Port 9 Transmit Strobe LVDS Positive
RXAstroben9	C10	Port 9 Transmit Strobe LVDS Negative
TXAdatap9	A11	Port 9 Receive Data LVDS Positive
TXAdatan9	B11	Port 9 Receive Data LVDS Negative
TXAstrobep9	C9	Port 9 Receive Strobe LVDS Positive
TXAstroben9	C8	Port 9 Receive Strobe LVDS Negative
RXAdatap10	G12	Port 10 Transmit Data LVDS Positive
RXAdatan10	G11	Port 10 Transmit Data LVDS Negative
RXAstrobep10	F10	Port 10 Transmit Strobe LVDS Positive
RXAstroben10	G10	Port 10 Transmit Strobe LVDS Negative
TXAdatap10	D11	Port 10 Receive Data LVDS Positive
TXAdatan10	D10	Port 10 Receive Data LVDS Negative
TXAstrobep10	H10	Port 10 Receive Strobe LVDS Positive
TXAstroben10	H9	Port 10 Receive Strobe LVDS Negative
RXAdatap11	B13	Port 11 Transmit Data LVDS Positive
RXAdatan11	B12	Port 11 Transmit Data LVDS Negative
RXAstrobep11	A8	Port 11 Transmit Strobe LVDS Positive
RXAstroben11	B8	Port 11 Transmit Strobe LVDS Negative
TXAdatap11	E11	Port 11 Receive Data LVDS Positive
TXAdatan11	F11	Port 11 Receive Data LVDS Negative
TXAstrobep11	A6	Port 11 Receive Strobe LVDS Positive
TXAstroben11	B6	Port 11 Receive Strobe LVDS Negative
RXAdatap12	H12	Port 12 Transmit Data LVDS Positive
RXAdatan12	J11	Port 12 Transmit Data LVDS Negative
RXAstrobep12	B7	Port 12 Transmit Strobe LVDS Positive
RXAstroben12	C7	Port 12 Transmit Strobe LVDS Negative
TXAdatap12	A10	Port 12 Receive Data LVDS Positive
TXAdatan12	A9	Port 12 Receive Data LVDS Negative
TXAstrobep12	F8	Port 12 Receive Strobe LVDS Positive
TXAstroben12	G8	Port 12 Receive Strobe LVDS Negative
RXAdatap13	AK29	Port 13 Transmit Data LVDS Positive
RXAdatan13	AJ29	Port 13 Transmit Data LVDS Negative
RXAstrobep13	AF28	Port 13 Transmit Strobe LVDS Positive
RXAstroben13	AE27	Port 13 Transmit Strobe LVDS Negative
TXAdatap13	AF26	Port 13 Receive Data LVDS Positive
TXAdatan13	AE26	Port 13 Receive Data LVDS Negative
TXAstrobep13	AN32	Port 13 Receive Strobe LVDS Positive
TXAstroben13	AN33	Port 13 Receive Strobe LVDS Negative
RXAdatap14	AK21	Port 14 Transmit Data LVDS Positive
RXAdatan14	AL21	Port 14 Transmit Data LVDS Negative
RXAstrobep14	AH28	Port 14 Transmit Strobe LVDS Positive
RXAstroben14	AH29	Port 14 Transmit Strobe LVDS Negative
TXAdatap14	AP30	Port 14 Receive Data LVDS Positive

TXAdatan14	AN30	Port 14 Receive Data LVDS Negative
TXAstrobep14	AG27	Port 14 Receive Strobe LVDS Positive
TXAstroben14	AG28	Port 14 Receive Strobe LVDS Negative
RXAdatap15	AM21	Port 15 Transmit Data LVDS Positive
RXAdatan15	AM22	Port 15 Transmit Data LVDS Negative
RXAstrobep15	AM30	Port 15 Transmit Strobe LVDS Positive
RXAstroben15	AL30	Port 15 Transmit Strobe LVDS Negative
TXAdatap15	AP27	Port 15 Receive Data LVDS Positive
TXAdatan15	AN27	Port 15 Receive Data LVDS Negative
TXAstrobep15	AP31	Port 15 Receive Strobe LVDS Positive
TXAstroben15	AP32	Port 15 Receive Strobe LVDS Negative
RXAdatap16	AK22	Port 15 Transmit Data LVDS Positive
RXAdatan16	AK23	Port 15 Transmit Data LVDS Negative
RXAstrobep16	AL28	Port 15 Transmit Strobe LVDS Positive
RXAstroben16	AL29	Port 15 Transmit Strobe LVDS Negative
TXAdatap16	AP25	Port 15 Receive Data LVDS Positive
TXAdatan16	AP26	Port 15 Receive Data LVDS Negative
TXAstrobep16	AJ27	Port 15 Receive Strobe LVDS Positive
TXAstroben16	AH27	Port 15 Receive Strobe LVDS Negative

ORDERING INFORMATION

UT200SpW16RTR-EVB:

UT *****



Device Type:
200SpW16RTR-EVB = SpaceWire Router Evaluation Board

|Aeroflex Colorado Springs - Datasheet Definition

Advanced Datasheet - Product In Development

Preliminary Datasheet - Shipping Prototype

Datasheet - Shipping QML & Reduced Hi-Rel

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Our passion for performance is defined by three attributes represented by these three icons: solution-minded, performance-driven and customer-focused