

# UT22VP10 Universal RADPAL™



November 2000

## FEATURES

- High speed Universal RADPAL
  - $t_{PD}$ : 15.5ns, 20ns, 25ns maximum
  - $f_{MAX1}$ : 33MHz maximum external frequency
  - Supported by industry-standard programmer
  - Amorphous silicon anti-fuse
- Asynchronous and synchronous RADPAL operation
  - Synchronous PRESET
  - Asynchronous RESET
- Up to 22 input and 10 output drivers may be configured
  - CMOS & TTL-compatible input and output levels
  - Three-state output drivers
- Variable product terms, 8 to 16 per output
- 10 user-programmable output macrocells
  - Registered or combinatorial operation
  - Output driver polarity control selectable
  - Two feedback paths available
- Radiation-hardened process and design; total dose irradiation testing to MIL-STD-883, Method 1019
  - Total dose: 1.0E6 rads(Si)
  - Upset threshold 50 MeV-cm<sup>2</sup>/mg (min)
  - Latchup immune(LET>109 MeV-cm<sup>2</sup>/mg)
- QML Q & V compliant
- Packaging options:
  - 24-pin 100-mil center DIP (0.300 x 1.2)
  - 24-lead flatpack (.45 x .64)
  - 28-lead quad-flatpack (.45 x .45)
- Standard Military Drawing 5962-94754 available

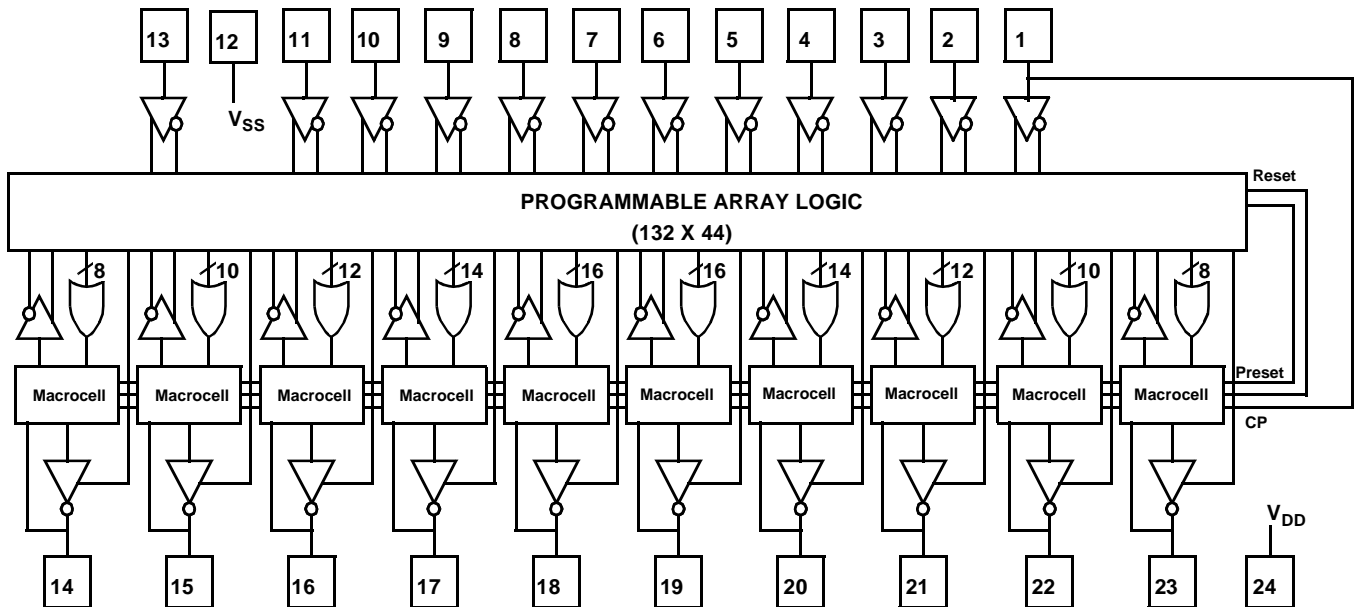


Figure 1. Block Diagram

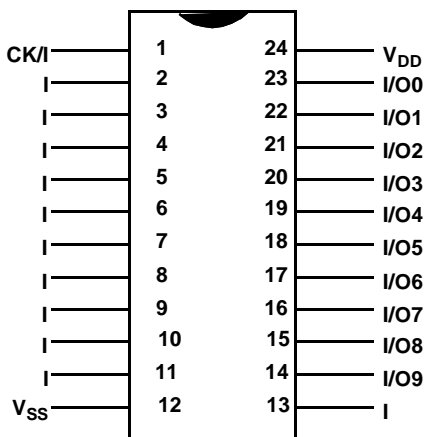
## PRODUCT DESCRIPTION

The UT22VP10 RADPAL is a fuse programmable logic array device. The familiar sum-of-products (AND-OR) logic structure is complemented with a programmable macrocell. The UT22VP10 is available in 24-pin DIP, 24-lead flatpack, and 28-lead quad-flatpack package offerings providing up to 22 inputs and 10 outputs. Amorphous silicon anti-fuse technology provides the programming of each output. The user specifies whether each of the potential outputs is registered or combinatorial. Output polarity is also individually selected, allowing for greater flexibility for output configuration. A unique output enable function allows the user to configure bidirectional I/O on an individual basis.

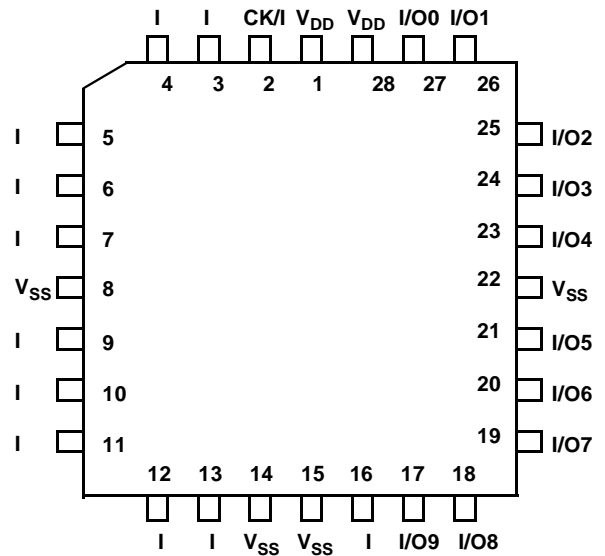
The UT22VP10 architecture implements variable sum terms providing 8 to 16 product terms to outputs. This feature provides the user with increased logic function flexibility. Other features include common synchronous preset and asynchronous reset. These features eliminate the need for performing the initialization function.

The UT22VP10 provides a device with the flexibility to implement logic functions in the 500 to 800 gate complexity. The flexible architecture supports the implementation of logic functions requiring up to 21 inputs and only a single output or down to 12 inputs and 10 outputs. Development and programming support for the UT22VP10 is provided by DATA I/O.

## DIP & FLATPACK PIN CONFIGURATION



## QUAD-FLATPACK PIN CONFIGURATION



## PIN NAMES

CK/I	Clock/Data Input
I	Data Input
I/O	Data Input/Output
V <sub>DD</sub>	Power
V <sub>SS</sub>	Ground

## FUNCTION DESCRIPTION

The UT22VP10 RADPAL implements logic functions as sum-of-products expressions in a one-time programmable-AND/fixed-OR logic array. User-defined functions are created by programming the connections of input signals into the array. User-configurable output structures in the form of I/O macrocells further increase logic flexibility.

**Table 1. Macrocell Configuration Table<sup>1, 2, 3</sup>**

<b>C<sub>2</sub></b>	<b>C<sub>1</sub></b>	<b>C<sub>0</sub></b>	<b>Output Type</b>	<b>Polarity</b>	<b>Feedback</b>
0	0	0	Registered	Active LOW	Registered
0	0	1	Registered	Active HIGH	Registered
X	1	0	Combinatorial	Active LOW	I/O
X	1	1	Combinatorial	Active HIGH	I/O
1	0	0	Registered	Active LOW	I/O
1	0	1	Registered	Active HIGH	I/O

**Notes:**

1. 0 equals programmed low or programmed.
2. 1 equals programmed high or unprogrammed.
3. X equals don't care.

**OVERVIEW**

The UT22VP10 RADPAL architecture (see figure 1) has 12 dedicated inputs and 10 I/Os to provide up to 22 inputs and 10 outputs for creating logic functions. At the core of the device is a one-time programmable anti-fuse AND array that drives a fixed OR array. With this structure, the UT22VP10 can implement up to 10 sum-of-products logic expressions.

Associated with each of the 10 OR functions is a macrocell which is independently programmed to one of six different configurations. The one-time programmable macro cells allow each I/O to create sequential or combinatorial logic functions with either Active-High or Active-Low polarity.

**LOGIC ARRAY**

The one-time programmable AND array of the UT22VP10 RADPAL is formed by input lines intersecting product terms. The input lines and product terms are used as follows:

44 input lines:

- 24 input lines carry the true and complement of the signals applied to the input pins
- 20 lines carry the true and complement values of feedback or input signals from the 10 I/Os

132 product terms:

- 120 product terms (arranged in 2 groups of 8, 10, 12, 14, and 16) used to form logic sums
- 10 output enable terms (one for each I/O)
- 1 global synchronous preset term
- 1 global asynchronous reset term

At each input-line/product-term intersection there is an anti-fuse cell which determines whether or not there is a logical connection at that intersection. A product term which is connected to both the true and complement of an input signal will always be logical zero, and thus will not effect the OR function that it drives. When there are no connections on a product term

a Don't Care state exists and that term will always be a logical one.

**PRODUCT TERMS**

The UT22VP10 provides 120 product terms that drive the 10 OR functions. The 120 product terms connect to the outputs in two groups of 8, 10, 12, 14, and 16 to form logical sums.

**MACROCELL ARCHITECTURE**

The output macrocell provides complete control over the architecture of each output. Configuring each output independently permits users to tailor the configuration of the UT22VP10 to meet design requirements.

Each I/O macrocell (see figure 2) consists of a D flip-flop and two signal-select multiplexers. Three configuration select bits controlling the multiplexers determine the configuration of each UT22VP10 macrocell (see table 1). The configuration select bits determine output polarity, output type (registered or combinatorial) and input feedback type (registered or I/O). See figure 3 for equivalent circuits for the macrocell configurations.

**OUTPUT FUNCTIONS**

The signal from the OR array may be fed directly to the output pin (combinatorial function) or latched in the D flip-flop (registered function). The D flip-flop latches data on the rising edge of the clock. When the synchronous preset term is satisfied, the Q output of the D flip-flop output will be set logical one at the next rising edge of the clock input. Satisfying the asynchronous clear term sets Q logical zero, regardless of the clock state. If both terms are satisfied simultaneously, the clear will override the preset.

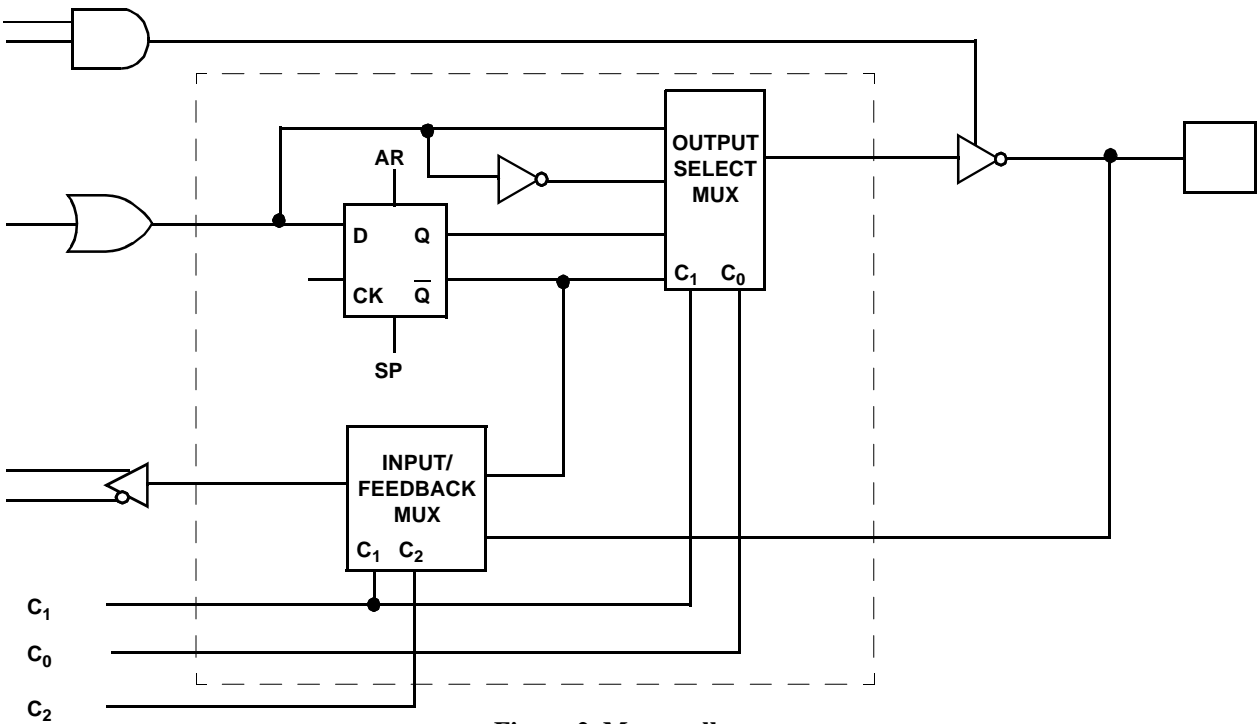


Figure 2. Macrocell

### OUTPUT POLARITY

Each macrocell can be configured to implement Active-High or Active-Low logic. Programmable polarity eliminates the need for external inverters.

### OUTPUT ENABLE

The output of each I/O macrocell can be enabled or disabled under the control a programmable output enable product term. The output signal is propagated to the I/O pin when the logical conditions programmed on the output enable term are satisfied. Otherwise, the output buffer is driven to the high-impedance state.

The output enable term allows the I/O pin to function as a dedicated input, dedicated output, or bidirectional I/O. When every connection is unprogrammed, the output enable product term permanently enables the output buffer and yields a dedicated output. If every connection is programmed, the enable term is logically low and the I/O functions as a dedicated input.

### REGISTER FEEDBACK

The feedback signal to the AND array is taken from the  $\bar{Q}$  output when the I/O macrocell implements a registered function ( $C_2 = 0, C_1 = 0$ ).

### BIDIRECTIONAL I/O

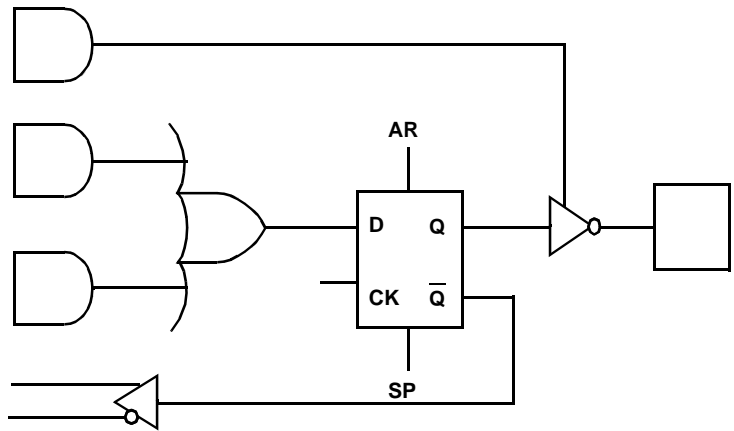
The feedback signal is taken from the I/O pin when the macrocell implements a combinatorial function ( $C_1 = 1$ ) or a registered function ( $C_2 = 1, C_1 = 0$ ). In this case, the pin can be used as a dedicated input, a dedicated output, or a bidirectional I/O.

### POWER-ON RESET

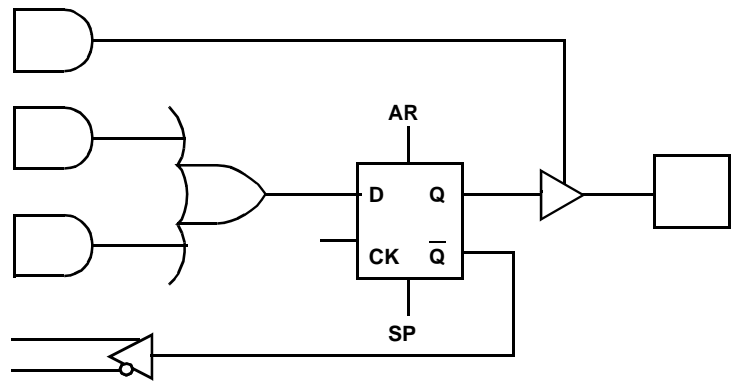
To ease system initialization, all D flip-flops will power-up to a reset condition and the Q output will be low. The actual output of the UT22VP10 will depend on the programmed output polarity. The reset delay time is 5 $\mu$ s maximum. See the Power-up Reset section for a more descriptive list of POR requirements.

### ANTI-FUSE SECURITY

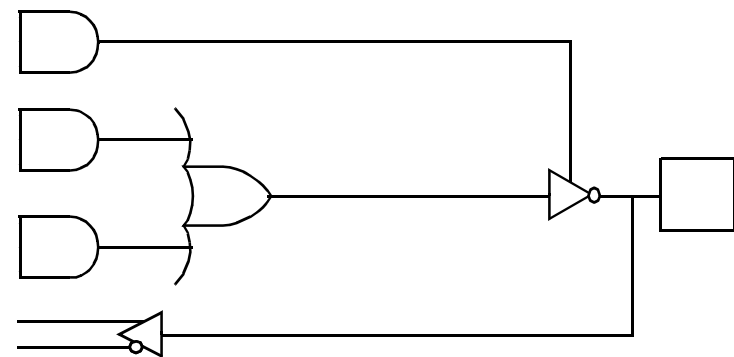
The UT22VP10 provides a security bit that prevents unauthorized reading or copying of designs programmed into the device. The security bit is set by the PLD programmer at the conclusion of the programming cycle. Once the security bit is set it is no longer possible to verify (read) or program the UT22VP10. **NOTE: UTMC does not recommend using the UT22VP10 unless the security fuse has been programmed. The security bit must be blown to ensure proper functionality of the UT22VP10.**



**Registered Feedback, Registered, Active-Low Output ( $C_2 = 0, C_1 = 0, C_0 = 0$ )**

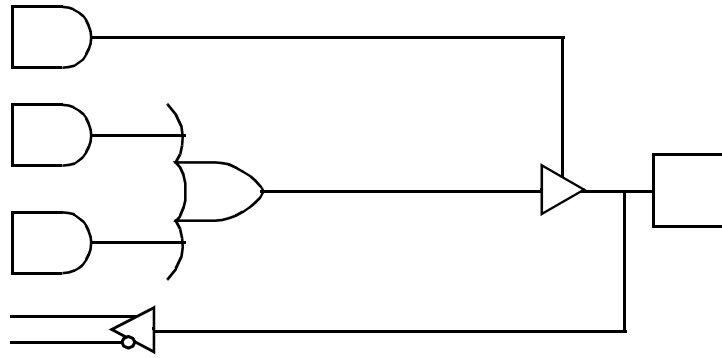


**Registered Feedback, Registered, Active-High Output ( $C_2 = 0, C_1 = 0, C_0 = 1$ )**

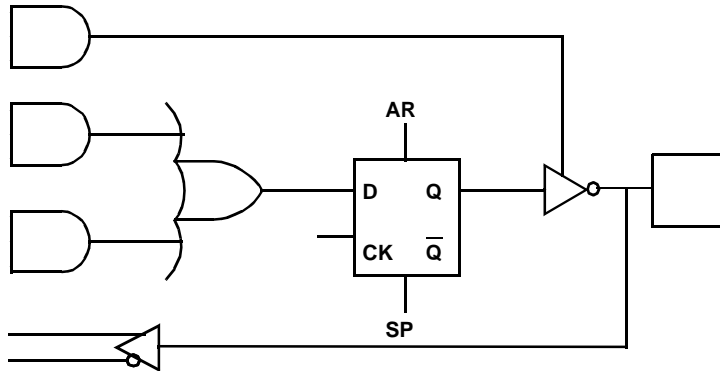


**I/O Feedback, Combinatorial, Active-Low Output ( $C_2 = X, C_1 = 1, C_0 = 0$ )**

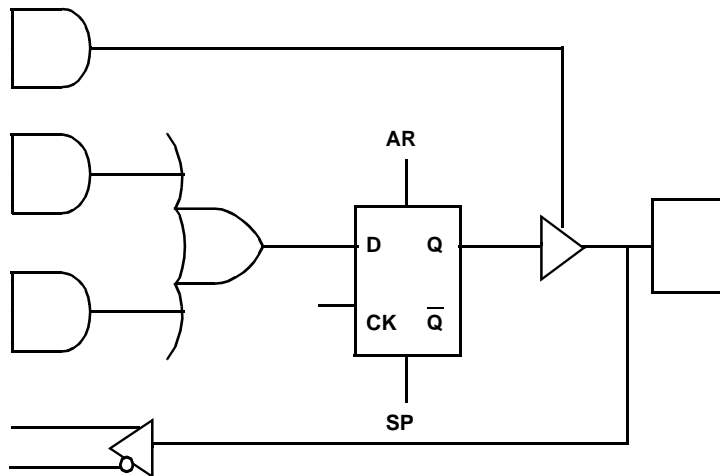
**Figure 3. Macrocell Configuration** (continued on next page)



**I/O Feedback, Combinatorial, Active-High Output ( $C_2 = X, C_1 = 1, C_0 = 1$ )**



**I/O Feedback, Registered, Active-Low Output ( $C_2 = 1, C_1 = 0, C_0 = 0$ )**



**I/O Feedback, Registered, Active-High Output ( $C_2 = 1, C_1 = 0, C_0 = 1$ )**

**Figure 3. Macrocell Configuration**

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

SYMBOL	PARAMETER	LIMIT	UNITS
$V_{DD}$	Supply voltage	-0.3 to 7.0	V
$V_{I/O}^2$	Input voltage any pin	-0.3 to +7.0	V
$T_{STG}$	Storage Temperature range	-65 to +150	°C
$T_J$	Maximum junction temperature	+175	°C
$T_S$	Lead temperature (soldering 10 seconds)	+300	°C
$\Theta_{JC}$	Thermal resistance junction to case	20	°C/W
$I_I$	DC input current	$\pm 10$	mA
$P_D^3$	Maximum power dissipation	1.6	W
$I_O$	Output sink current	12	mA

### Notes:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Minimum voltage is  $-0.6V_{DD}$  which may undershoot to  $-2.0V_{DD}$  for pulses of less than 20ns. Maximum output pin voltage is  $V_{DD} + 0.75V_{DD}$  which may overshoot to  $+7.0V_{DD}$  for pulses of less than 20ns.
3.  $(I_{CC} \text{ max} + I_{OS}) 5.5V$ .

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMIT	UNITS
$V_{DD}^1$	Supply voltage	4.5 to 5.5	V
$V_{IN}$	Input voltage any pin	0 to $V_{DD}$	V
$T_C$	Temperature range	-55 to +125	°C

### Notes:

1. See page 12 for minimum  $V_{DD}$  requirements at power-up.

## DC ELECTRICAL CHARACTERISTICS <sup>1,7</sup>

( $V_{DD}^2 = 5.0V \pm 10\%$ ;  $V_{SS} = 0V^3$ ,  $-55^\circ C < T_C < +125^\circ C$ )

SYMBOL	PARAMETER	CONDITION	MINIMUM	MAXIMUM	UNIT
$V_{IL}$	Low-level input voltage	TTL	--	.8	V
$V_{IH}$	High-level input voltage	TTL	2.2	--	V
$V_{IL}$	Low-level input voltage	CMOS	--	.3* $V_{DD}$	V
$V_{IH}$	High-level input voltage	CMOS	.7* $V_{DD}$	--	V
$V_{OL}$	Low-level output voltage	$I_{OL} = 12.0mA$ , $V_{DD} = 4.5V$ (TTL)		.4	V
$V_{OH}$	High-level output voltage	$I_{OH} = -12.0mA$ , $V_{DD} = 4.5V$ (TTL)	2.4	--	V
$V_{OL}$	Low-level output voltage	$I_{OL} = 200mA$ , $V_{DD} = 4.5V$ (CMOS)	--	$V_{SS}+0.05$	V
$V_{OH}$	High-level output voltage	$I_{OH} = -200mA$ , $V_{DD} = 4.5V$ (CMOS)	$V_{DD}-0.05$	--	V
$I_{IN}$	Input leakage current	$V_{IN} = V_{DD}$ and $V_{SS}$	-10	10	$\mu A$
$I_{OZ}$	Three-state output leakage current	$V_O = V_{DD}$ and $V_{SS}$ , $V_{DD} = 5.5V$	-10	10	$\mu A$
$I_{OS}^{4,5}$	Short-circuit output current	$V_{DD} = 5.5V$ , $V_O = V_{DD}$ $V_{DD} = 5.5V$ , $V_O = 0V$	-160	160	mA
$C_{IN}^{5,6}$	Input capacitance	$f_i = 1MHz$ @0V	--	15	pF
$C_{I/O}^{5,6}$	Bidirectional capacitance	$f_i = 1MHz$ @0V	--	15	pF
$I_{DD}^5$	Supply current: Output three-state, worst-case pattern programmed, $f_i = f_{MAX1}$	$V_{DD} = 5.5V$	--	120	mA
$I_{DDQ}$	Supply current: Unprogrammed	$V_{DD} = 5.5V$	--	25	mA

### Notes:

1. All specifications valid for radiation dose  $\leq 1E6$  rads(Si).
2. See page 12 for minimum  $V_{DD}$  requirements at power-up.
3. Maximum allowable relative shift equals 50mV.
4. Duration not to exceed 1 second, one output at a time.
5. Tested initially and after any design or process changes that affect that parameter and, therefore, shall be guaranteed to the limit specified.
6. All pins not being tested are to be open.
7. CMOS levels only tested on CMOS devices. TTL levels only tested on TTL devices.

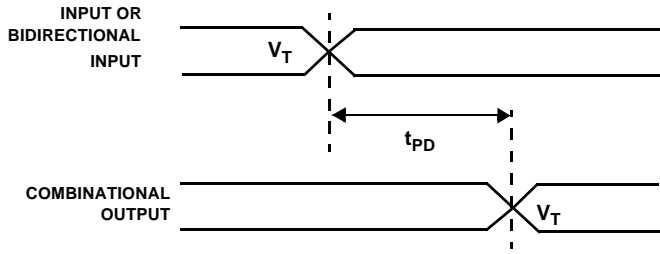
## AC CHARACTERISTICS READ CYCLE (Post-Radiation) <sup>1,2</sup>

( $V_{DD}^3 = 5.0V \pm 10\%$ ;  $-55^\circ C < T_C < +125^\circ C$ )

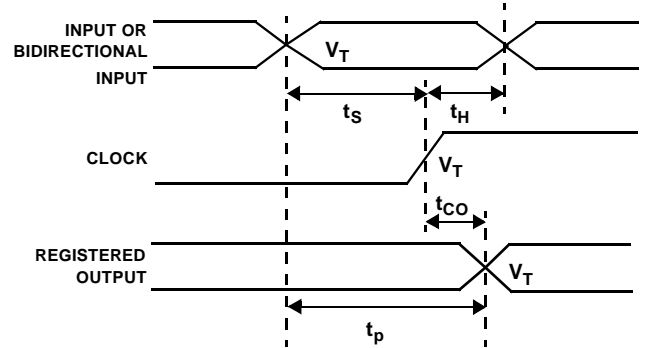
SYMBOL	PARAMETER	22VP10-15.5		22VP10-20		22VP10-25		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PD}^{4,5,6}$	Input to output propagation delay		15.5		20		25	ns
$t_{EA}^4$	Input to output enable delay		23		23		25	ns
$t_{ER}^4$	Input to output disable delay		23		23		25	ns
$t_{CO}^{4,6}$	Clock to output delay		15		15		15	ns
$t_{CO2}^4$	Clock to combinatorial output delay via internal registered feedback		24		24		28	ns
$t_S^{4,6}$	Input or feedback setup time	15		15		18		ns
$t_H^{4,6}$	Input or feedback hold time	2		2		2		ns
$t_P^4$	External clock period ( $t_{CO} + t_S$ )	30		30		33		ns
$t_{WH, WL}^4$	Clock width, clock high time, clock low time	12		12		14		ns
$f_{MAX1}^{4,6}$	External maximum frequency ( $1/(t_{CO} + t_S)$ )		33		33		30	MHz
$f_{MAX2}^{4,6}$	Data path maximum frequency ( $1/(t_{WH} + t_{WL})$ )		42		42		36	MHz
$f_{MAX3}^{4,6}$	Internal feedback maximum frequency ( $1/(t_{CO} + t_{CF})$ )		32		32		32	MHz
$t_{CF}^4$	Register clock to feedback input		13		13		13	ns
$t_{AW}^4$	Asynchronous reset width	20		20		25		ns
$t_{AR}^4$	Asynchronous reset recovery time	20		20		25		ns
$t_{AP}^4$	Input to asynchronous reset		20		20		25	ns
$t_{SPR}^{4,6}$	Synchronous preset recovery time	20		20		25		ns
$t_{PR}^{4,6}$	Power up reset time	1.0		1.0		1.0		$\mu s$

### Notes:

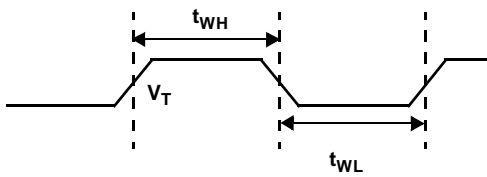
1. Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019 at 1.0E6 rads(Si).
2. Guaranteed by characterization.
3. See page 12 for minimum  $V_{DD}$  requirements for power-up.
4. Tested initially and after any design or process changes that affect.
5. Device 22VP10-15 tested at -55°C, +25°C and +50°C. At 125°C, tested to 20ns limit.
6. Tested on Programmed Test Ring only.



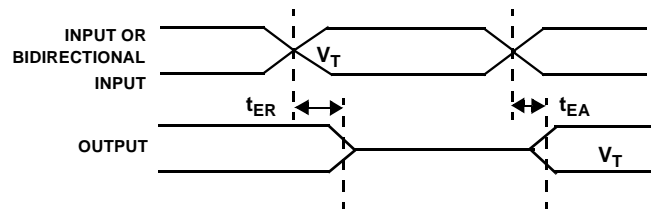
Combinatorial Output



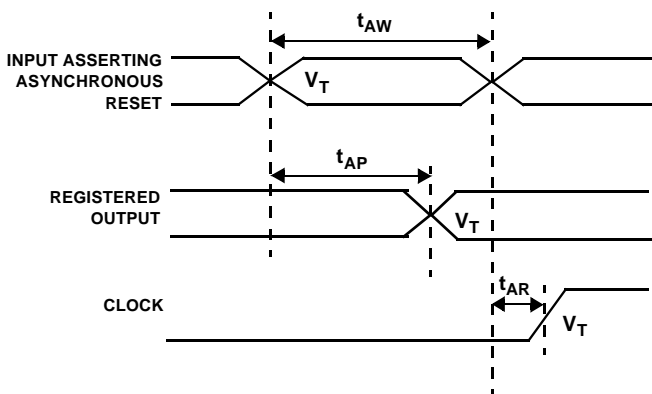
Registered Output



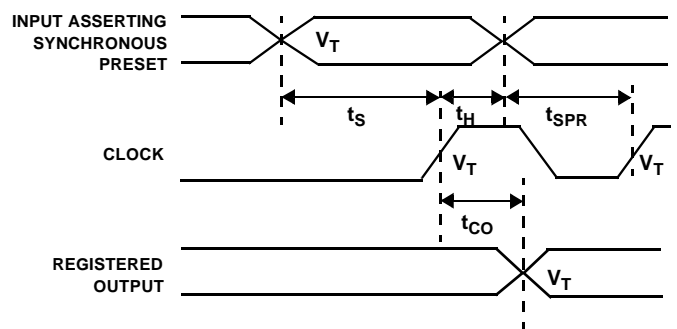
Clock Width



Combinatorial Output  
( $V_{OH} - 0.5V, V_{OL} + 0.5V$ )



Asynchronous Reset

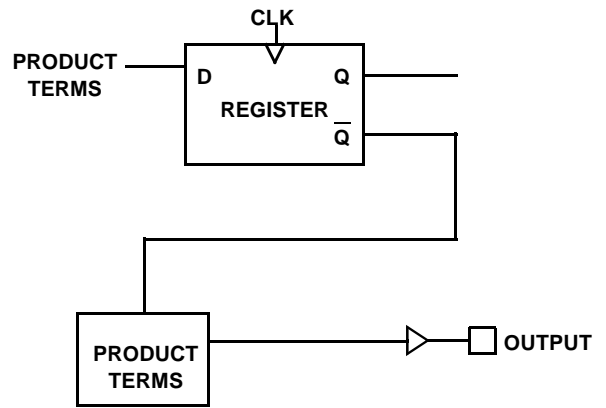
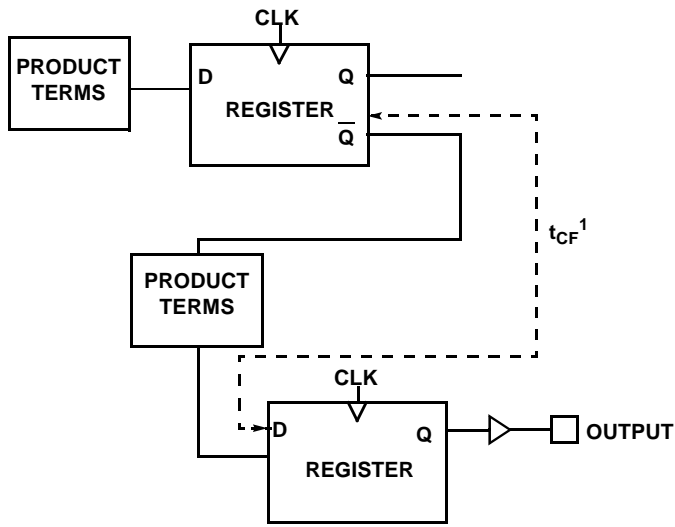


Synchronous Preset

Notes:

1.  $V_T = 1.5V$ .
2. Input pulse amplitude 0V to 3.0V.
3. Input rise and fall times 3ns maximum.

Figure 4. AC Electrical<sup>1,2,3</sup>



**Clock to Combinatorial Output ( $t_{CO2}$ )**

**Note:**

1.  $t_{CF}$  defined as the propagation delay from  $\bar{Q}$  to D register input.

$$f_{MAX3}: \text{Internal Feedback} \left( \frac{1}{t_{CO} + t_{CF}} \right)$$

**Figure 5. Signal Paths**

## POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will depend on the programmed pattern. This feature is valuable in simplifying state machine initialization. See figure 6 for a timing diagram. Due to the synchronous operation of the power-up reset and the wide range of ways  $V_{DD}$  can rise to its steady state, the following five conditions are required to ensure a valid power-up reset.

1. The voltage supplied to the  $V_{DD}$  pin(s) must be equal to 0V prior to the intended power-up sequence.
2. The voltage on  $V_{DD}$  must rise from 0V to 1V at a rate of 0.1V/s or faster.
3. The  $V_{DD}$  rise must be continuously increasing with respect to time, through 3V, and monotonic thereafter.

4. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.
5. The power-up voltage must meet the minimum  $V_{DD}$  requirements described by the following device dependent and temperature dependent equations:

SMD Device types 01, 02, 03, 04, 08      CMOS and TTL  
 $V_{DD} = 4.61V - 0.0090 * (^{\circ}C)$   
 SMD Device types 05, 06, 07      CMOS  
 $V_{DD} = 4.41 - 0.0090 * (^{\circ}C)$

**Note: The minimum  $V_{DD}$  requirement above is not applicable if the UT22VP10 application is purely combinatorial (i.e. no registered outputs).**

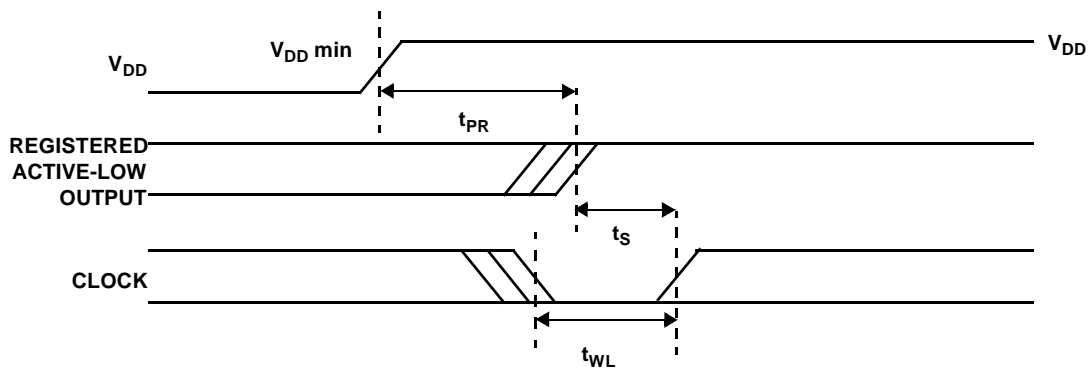


Figure 6. Power-Up Reset Waveform

## RADIATION HARDNESS

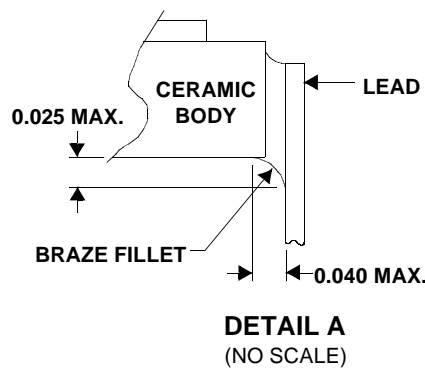
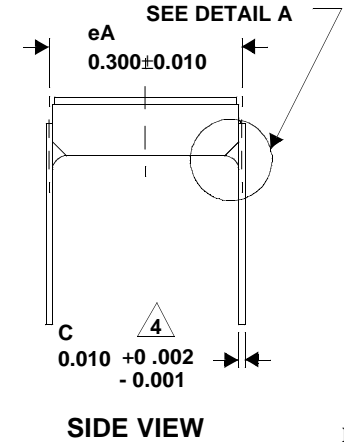
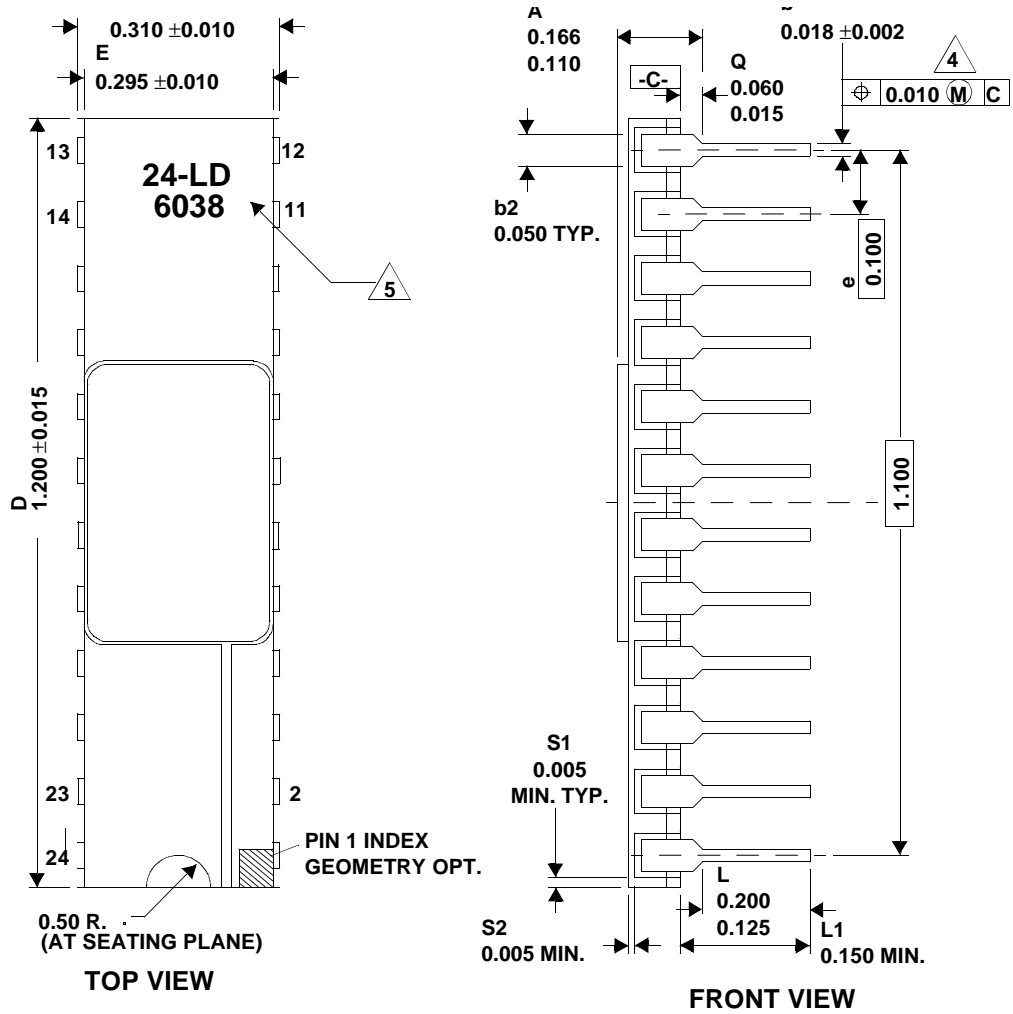
The UT22VP10 RADPAL incorporates special design and layout features which allow operation in high-level radiation environments. UPMC has developed special low-temperature processing techniques designed to enhance the total-dose radiation hardness of both the gate oxide and the field oxide while maintaining the circuit density and reliability. For transient radiation hardness and latchup immunity, UPMC builds radiation-hardened products on epitaxial wafers using an advanced twin-tub CMOS process.

## RADIATION HARDNESS DESIGN SPECIFICATIONS<sup>1</sup>

PARAMETER	CONDITION	MINIMUM	UNIT
Total Dose	+25°C per MIL-STD-883 Method 1019	1.0E6	rads(Si)
LET Threshold	-55°C to +125°C	50	MeV-cm <sup>2</sup> /mg
Neutron Fluence	1MeV equivalent	1.0E14	n/cm <sup>2</sup>

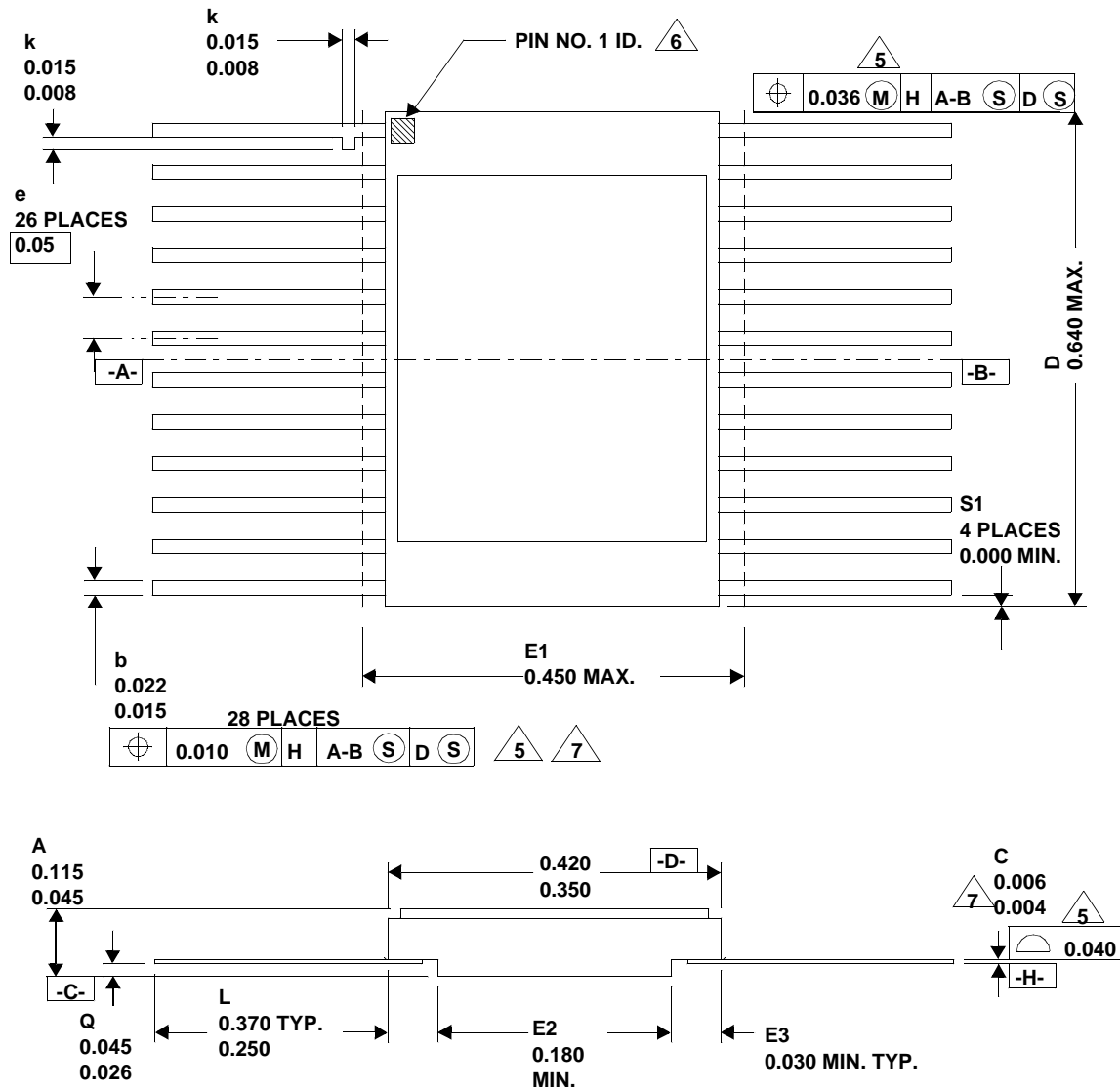
**Note:**

1. The RADPAL will not latchup during radiation exposure under recommended operating conditions.



- Notes:**
1. Package material: Opaque ceramic.
  2. All exposed metalized areas are finished per MIL-PRF-38535.
  3. Letter designations are for cross-reference to MIL-STD-1835.
  4. For solder coated leads, increase maximum limit by 0.003 inch as measured at the center of the flat.
  5. Numbering and lettering on the ceramic are not subject to visual marking criteria.

**Figure 7. 24-Pin 100-mil Center DIP (0.300 x 1.2)**



**Notes:**

1. All exposed metalized areas are gold plated over electroplated nickel per MIL-PRF-38535.
2. The lid is electrically connected to  $V_{SS}$ .
3. Lead finishes are in accordance with MIL-PRF-38535.
4. Dimension letters refer to MIL-STD-1835.
- $\triangle 5$  Lead position and coplanarity are not measured.
- $\triangle 6$  ID mark symbol is vendor option.
- $\triangle 7$  For solder coated leads, increase maximum limit by 0.003 inch as measured at the center of the flat.

**Figure 8. 24-Lead Flatpack (0.45 x 0.64)**

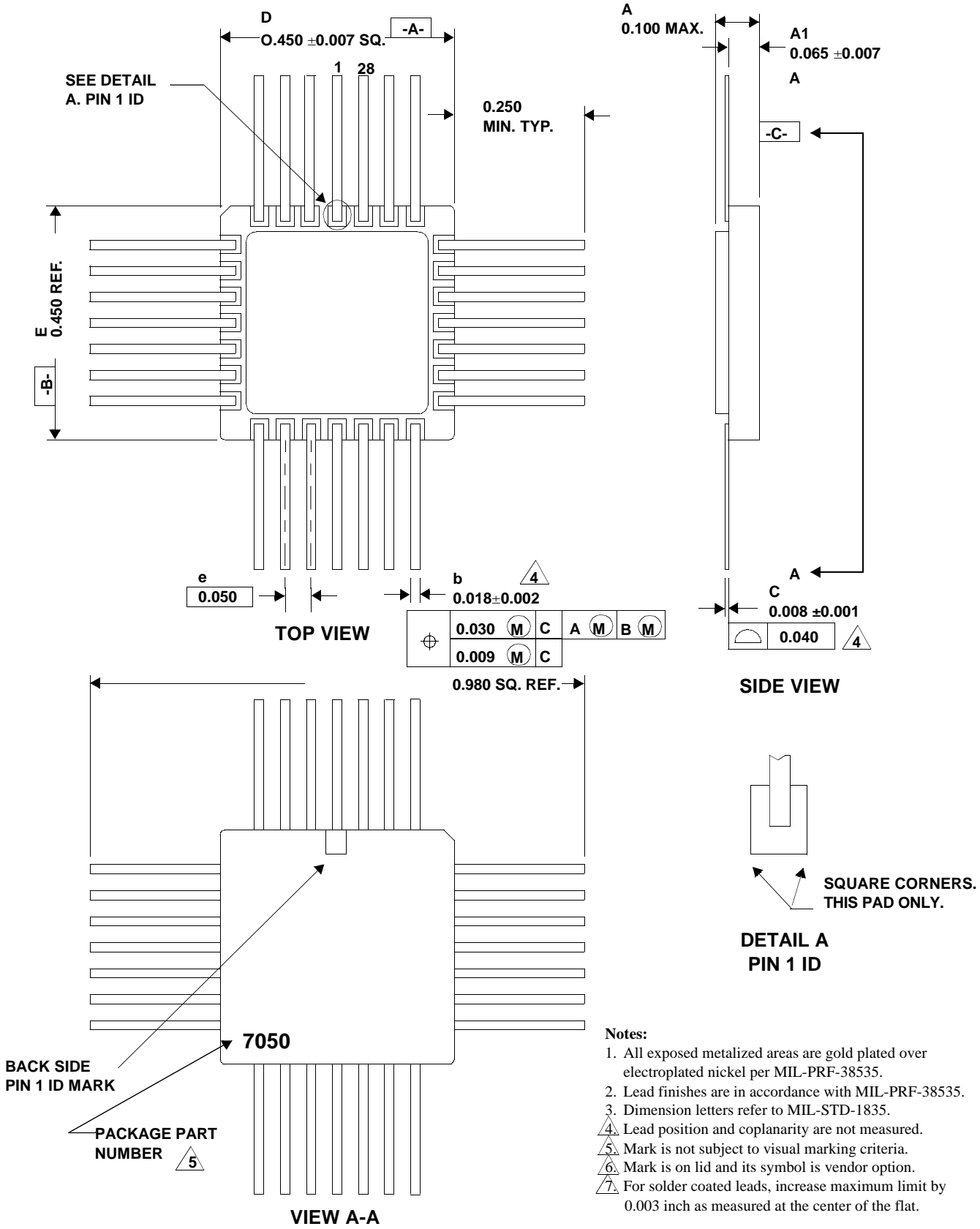
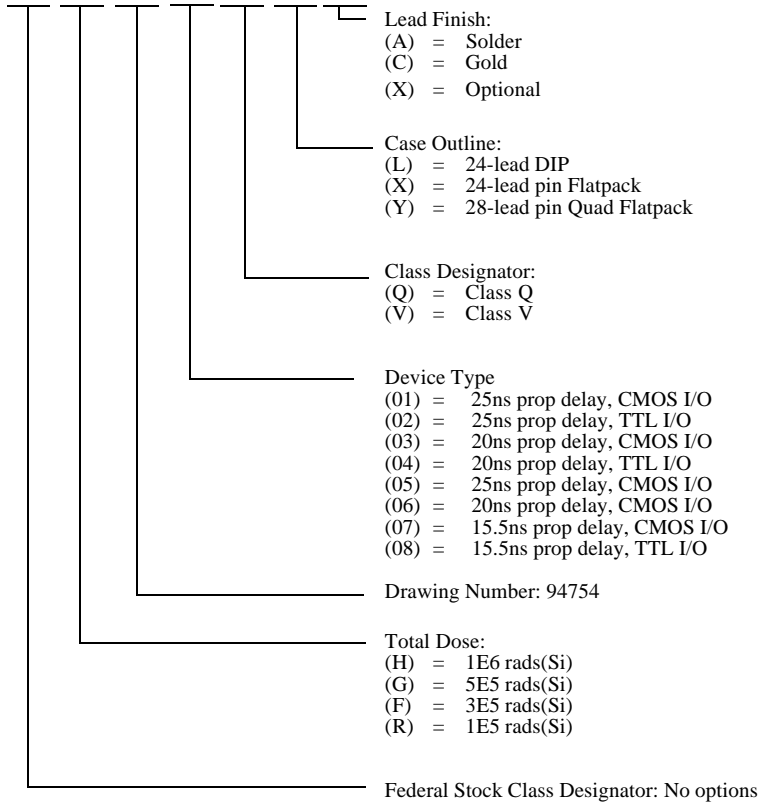


Figure 9. 28-Lead Quad-Flatpack (.45 x .45)

# ORDERING INFORMATION

## UT22VP10 Radiation Hardened PAL: SMD

5962 \* 94754 \* \* \* \*

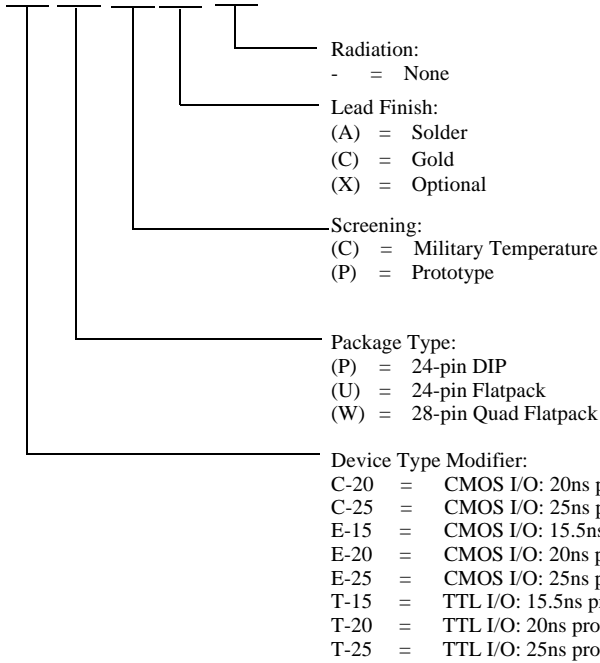


### Notes:

1. Lead finish (A, C, or X) must be specified.
2. If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening.
4. (01-04, 08) is  $V_{DD}(\min) = -0.009(^{\circ}\text{C})+4.61$ .
5. (05-07) is  $V_{DD}(\min) = -0.009(^{\circ}\text{C})+4.41$ .
6. (07, 08) is tested at  $-55^{\circ}\text{C}$ ,  $+25^{\circ}\text{C}$ , and  $+50^{\circ}\text{C}$  to 15.5ns for  $t_{PD}$ . At  $+125^{\circ}\text{C}$  tested to 20ns limit for  $t_{PD}$ .

## UT22VP10 Radiation Hardened PAL

UT22VP10 \* \* \* \* \*



### Notes:

1. Lead finish (A, C, or X) must be specified.
2. If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Military Temperature range flow per UTMC's manufacturing flows document. Devices have 48 hours of burn-in and are tested at -55°C, room temperature, and 125°C. Radiation characteristics are neither tested nor guaranteed and may not be specified.
4. Prototype flow per UTMC Manufacturing Flows Technical Description. Devices have prototype assembly and are tested at 25°C only. Radiation is neither tested nor guaranteed.
5. (T-15, C-25, T-25, C-20, T-20) is  $V_{DD}(\min) = -0.009*(^{\circ}C)+4.61$ .
6. (E-15, E-20 and E-25) is  $V_{DD}(\min) = -0.009*(^{\circ}C)+4.41$ .
7. (E-15 and T-15) is tested at at -55°C, +25°C, and +50°C to 15.5ns for  $t_{PD}$ . At +125°C tested to 20ns limit for  $t_{PD}$ .

# APPENDIX A

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## UT22VP10 RADPAL Power-On-Reset Ramp Rate Anomaly

UTMC has identified the following anomaly in the power up behavior of the UT22VP10 RAD<sub>PAL</sub> (RC01 and RC02).

### Anomaly:

The anomaly was observed for a power-up application where a residual voltage between 200 and 500 mV was supplied to the  $V_{DD}$  pin(s) of the RAD<sub>PAL</sub> for several milliseconds prior to the 5V power supply ramping to 5 volts. Consequently, the RAD<sub>PAL</sub> enters a “test” mode (as opposed to a “user” mode). In the test mode, all output buffers are placed and remain in a high impedance state and the RAD<sub>PAL</sub> does not function as programmed.

Through HSPICE simulation and laboratory tests, UTMC has found there exists a window in which a residual voltage of a few hundred millivolts on the  $V_{DD}$  pin(s) prevents the RAD<sub>PAL</sub> from generating an internal POR signal for its security circuit. The lack of a reset signal allows the security circuit to power up in either the “user” or the “test” mode of operation. Entering the “test” mode prevents the RAD<sub>PAL</sub> from functioning as programmed. The anomaly is seen at room temperature and above, where a residual voltage above 200mV is applied to  $V_{DD}$  before it transitions to  $V_{DD}$  minimum. The anomaly is ~~not seen~~ when the application of power to the RAD<sub>PAL</sub> starts at zero volts and transitions monotonically to  $V_{DD}$  minimum and the slew rate is greater than 0.1V/S.

The anomaly is not wafer lot dependent and affects all date code shipped.

### Solution:

The UT22VP10 RAD<sub>PAL</sub> is susceptible to this POR anomaly whenever residual voltages of between 200mV and 500mV are on the  $V_{DD}$  pin(s) prior to the application of the 5V power supply.

In order to avoid powering up the UT22VP10 RAD<sub>PAL</sub> into a test mode, the following specifications must be met:

- 1) The application of voltages on the  $V_{DD}$  pin(s) of the RAD<sub>PAL</sub> ~~must~~ start at 0V and reach 1V at a rate of 0.1V/s or faster.
- 2) The power-up voltage must be ~~continuously increasing~~ with respect to time, through 3V, and monotonic thereafter.
- 3) No voltage can be applied to  $V_{DD}$  prior to the intended power-up sequence.

An alternative or additional method to guarantee that the UT22VP10 RAD<sub>PAL</sub> functions in the user mode of operation is to implement the following fix into the board level design:

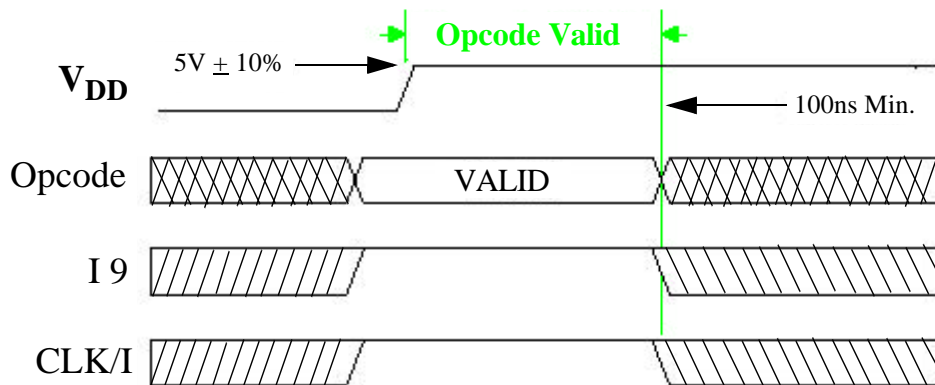
- 1) Apply one of the opcodes shown in Table 1 to the corresponding inputs of the RAD<sub>PAL</sub>. Notice that the Clock and I9 inputs must have a logic “1” applied during the application of a valid opcode.

**Table 1: Valid Power-Up Opcodes**

Mode of Operation	Power-Up Opcode (HEX) <sup>1</sup>	RAD <sub>PAL</sub> Input Pins									
		I9	I8	I7	I6	I5	I4	I3	I2	I1	Clk/I
0	DC	1	1	1	0	1	1	1	0	0	1
2	DE	1	1	1	0	1	1	1	1	0	1
3	DF	1	1	1	0	1	1	1	1	1	1
4	E0	1	1	1	1	0	0	0	0	0	1
5	E1	1	1	1	1	0	0	0	0	1	1
6	E2	1	1	1	1	0	0	0	1	0	1

Notes: 1. The Hexadecimal power-up opcode refers to the RAD<sub>PAL</sub> inputs I8 - I1.

- 2) Apply one of the opcodes from Table 1 for at least 100ns anytime after  $V_{DD}$  is within  $5V \pm 10\%$  to ensure all test mode latches are cleared. Figure 1 shows the opcode timing diagram.



**Figure 1. Opcode Timing**

Applying one of the opcodes from Table 1 enables the programmed security fuse to reset the internal test latch, forcing the UT22VP10 RAD<sub>PAL</sub> into the user mode of operation.

## APPENDIX B

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### **RADPAL™ Power-On-Reset Performance at Cold Temperatures**

UTMC has identified the following anomaly in the power up behavior of the UT22VP10 RADPAL™.

#### **Anomaly:**

The anomaly was observed for power-up applications where the voltage applied to the  $V_{DD}$  pin(s) of the RADPAL™ was within the specified voltage tolerance of  $5V \pm 10\%$ , yet, was not sufficient to turn off the internal reset pulse at cold temperature. Consequently, all programmed macro-cells would remain in reset until the power supply reached a minimum voltage.

UTMC has characterized this anomaly through HSPICE simulation, and laboratory testing. The characterization data shows that the minimum power-up voltage dependency on temperature fits a linear curve. Additionally, UTMC has identified distinct wafer lots that contain die with better cold temperature performance than the original supply of die. The wafer characterization is performed in the following manner:

- 1) Each wafer is evaluated for the transistor threshold voltages.
- 2) Each wafer showing satisfactory threshold voltages is then mapped to find die that have a high probability of representing the typical threshold voltage found across the wafer.
- 3) These selected die are then packaged, programmed, and characterized.
- 4) The test process ramps the voltage on the  $V_{DD}$  pin(s) of the RADPAL™ and measures the minimum voltage required for the reset signal to turn off.
- 5) These voltage measurements are taken in five degree increments in temperature through  $-55^{\circ}\text{C}$ .
- 6) The characterization data is then plotted to verify that the samples fit the specified  $V_{DD}$  to temperature curve.

As a result of the characterization performed, UTMC has developed the following equations that UT22VP10 RADPAL™ device types will satisfy:

- 1) SMD device types 01, 02, 03, 04 (CMOS and TTL) satisfy

$$V_{DD} = 4.61V - 0.0090 * (\text{Temperature } ^{\circ}\text{C})$$

- 2) SMD device types 05, 06 (CMOS only) satisfy

$$V_{DD} = 4.41V - 0.0090 * (\text{Temperature } ^{\circ}\text{C})$$

**Solution:**

To insure that the UT22VP10 RADPAL™ will power up in a usable mode, the following conditions must be met:

- 1) The voltage supplied to the  $V_{DD}$  pin(s) must be equal to 0V prior to the intended power-up sequence.
- 2) The voltage on  $V_{DD}$  must rise from 0V to 1V at a rate of 0.1V/s or faster.
- 3) The  $V_{DD}$  rise must be continuously increasing with respect to time, through 3V, and monotonic thereafter.
- 4) Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.
- 5) The power-up voltage must meet the minimum  $V_{DD}$  requirements described by the above device dependent equations. The customer can procure the specific device types meeting the respective equation via the SMD#5962-94754.

**NOTE: The minimum  $V_{DD}$  requirement above is not applicable if the UT22VP10 application is purely combinatorial (i.e. no outputs are registered)**