Application Note

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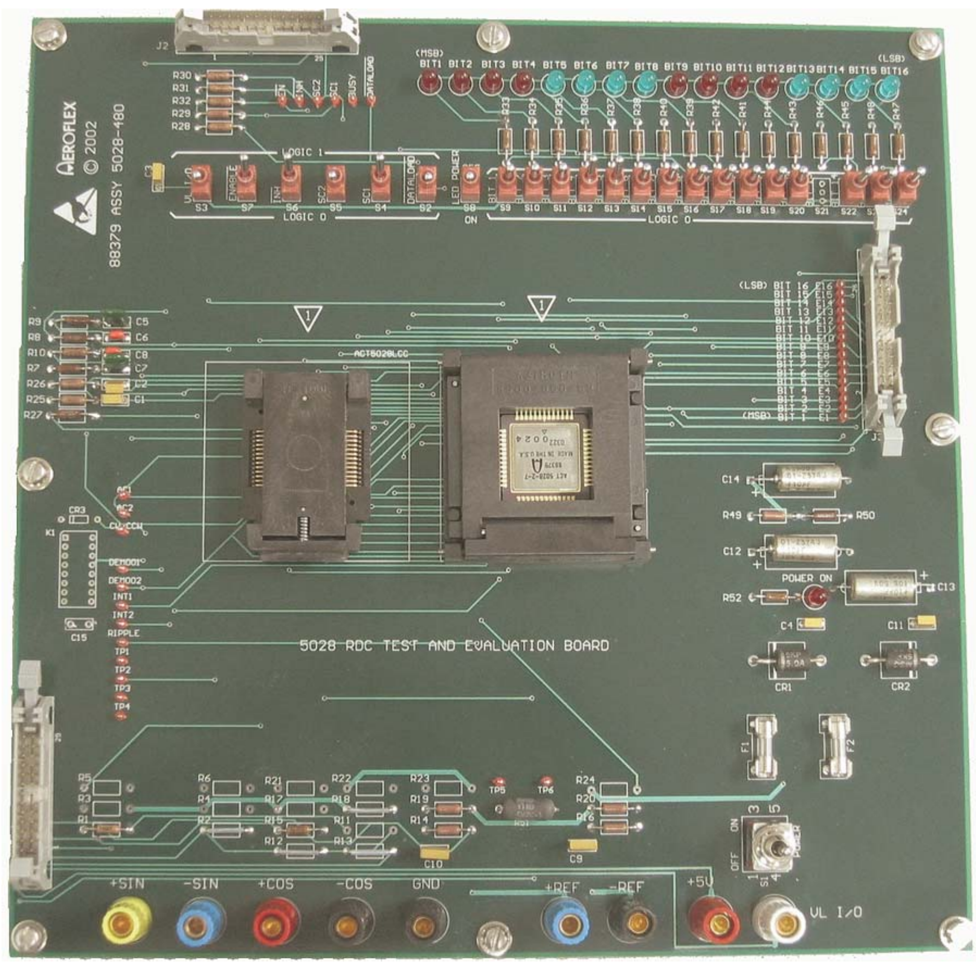
ACT5028 Resolver-To-Digital Converter (RDC) Evaluation Board



Scope:

This application note is to aid in the support of testing and evaluation of the ACT5028 Resolver to Digital (RDC) Converter on the ACT5028 Evaluation board developed by Aeroflex.

The Resolver inputs can be from an actual Resolver or a simulator as noted in Support Equipment below.

Support Documentation:

a) ACT5028 Product Data Sheet
b) 5028-411 Schematic of Evaluation Board
c) 5028-480 Evaluation Board Assembly
d) SW5028-2 Software Program to determine RDC bandwidth component values

Support Equipment Required:

a) +5 Volt Power Supply capable of .25amps
b) +5 to +3 Volt Power Supply if required for $VL_{I/O}$
c) Sine Wave Generator capable of 20 KHz @ 3 Volts RMS
d) North Atlantic Industry Synchro / Resolver Simulator Model 5330 or equivalent
e) Digital Multi Meter (Measure voltage, current, resistance, & capacitance)
f) Digital Oscilloscope

Connector Inputs:

J1	Used for Auto Test (Resolver Signals)
J2	Used for Auto Test (Control Signals)
J3	Used for Auto Test (Data Bus)
K1	Used for Auto Test (Power Relay)
+SIN	+SIN input signal from Resolver
-SIN	-SIN input signal from Resolver
+COS	+COS input signal from Resolver
-COS	-COS input signal from Resolver
+REF	+REF input signal from sine wave generator
-REF	-REF input signal from sine wave generator
+5V	System Power Supply
$VL_{I/O}$	Alternate Digital Interface Power (5-3.3Volts)
GND	System Ground

Controls:

S1 Power on switch (ON/OFF) for +5 V & $VL_{I/O}$ inputs

S2 DATALOAD; Loads the contents of the Data Bus into the RDC Converter
*Logic 0 No Load
*Logic 1 Load Data
*Note: Rev B Silicon has a reverse polarity

S3 $VL_{I/O;}$ Digital Logic Interface voltage
Logic 0 selects +5 Volts
Logic 1 selects $VL_{I/O}$ input

S4 SC1; Mode Select
S5 SC2;

SC1/S4	SC2/S5	
0	0	10 Bit Mode
0	1	12 Bit Mode
1	0	14 Bit Mode
1	1	16 Bit Mode

S6 $\overline{INH}$;
Logic 0 Inhibits Data Bus from changing
Logic 1 Enables Data Bus changes

S7 $\overline{ENABLE}$;
Logic 0 Enables Data Bus as an Output Port
Logic 1 Disables Data Bus output, HiZ State

S8 LED POWER (ON/OFF)

S9-24 Data Bus; Note care should be taken when driving the Data Bus, $\overline{ENABLE}$ should be at Logic 1.
Logic 0 selects a low logic level
Logic 1 selects a Hi logic level
Center position provides a HiZ state from the switch

LEDs:

Power On LED indicates that +5 Volts is turned on by S1.

Bit1-Bit16 Indicates the status of the corresponding Data bit on the Bus.

Electronic Components TBD:

Resolver Characteristics

R7-R10	Resistor Values TBD, 1/8w, 1%
R27	Resistor Values TBD, 1/8w, 1%
C5-C8	Ceramic Capacitor TBD, 25 Volt, 5%

Input Conditioning

R1-R4	Resistor Values TBD, 1/8w, 1%
R13-R20	Resistor Values TBD, 1/8w, 1%
C9-C10	Ceramic Capacitor TBD, 25 Volt, 5%

Evaluation Board Setup:

Determine System Characteristics:

All of the loop components (resistors & capacitors) are calculated for you in a convenient program, simply input the following information in the program. The reference designations in the program do not match the Evaluation Board, they reference the ACT5028 Product Data Sheet.

ACT5028 Evaluation Bd		Product Data Sheet
R10	same as	R3
R8 = R27	same as	R1
R7 = R9	same as	R2
C6 = C8	same as	C2
C5 = C7	same as	C3

Program Inputs:

a) Resolution
b) Maximum Tracking Rate
c) Closed Loop Bandwidth BW_{CL}
d) Carrier Frequency
e) SIN & COS input levels

Resolution	Select 10 for .35° (10 Bit Mode)
(Also configure SC1	Select 12 for .09° (12 Bit Mode)
& SC2 Switches on PCB)	Select 14 for .022° (14 Bit Mode)
	Select 16 for .0055° (16 Bit Mode)
Maximum	0 to 1024 RPS for 10 Bit Mode
Tracking Rate	0 to 256 RPS for 12 Bit Mode
	0 to 64 RPS for 14 Bit Mode
	0 to 16 RPS for 16 Bit Mode
Closed Loop Bandwidth	Typically > 10x Maximum Tracking Rate
Carrier Frequency	Range 45 to 30KHZ
(Supplied by user)	Must be > 4 x BW_{CL} in 10 Bit Mode
	Must be > 8 x BW_{CL} in 12 Bit Mode
	Must be > 12 x BW_{CL} in 14 Bit Mode
	Must be > 16 x BW_{CL} in 16 Bit Mode
SIN & COS Input	1 to 1.5 Vrms
(Supplied by user)	

Input Signal Conditioning:

The first decision is to select Single Ended or Differential input conditioning, Figure 1 shows the circuit components that must be selected. To maintain the best accuracy resistor tolerance and matching will be important. The input amplitude is not as important (staying within recommended input range) as maintaining matched amplitudes on the SIN and COS and when using differential inputs, symmetry should be maintained. Note the resistor reference designations in Figure 1 are grouped by A, B, C and D. Each group will have the same value and should be matched as close as possible. If no attenuation is required in the SIN / COS inputs, resistor group A is replaced with zero ohm jumper wires. If no attenuation is required for the Reference input, resistor group C would be replaced with zero ohm jumper wires.

Reference Input Conditioning:

Most Resolvers have a LEADING input to output phase shift. A simple C-R leading phase shift network from the Resolver reference to the RDC's reference input will provide the compensating phase shift required to bring the signals in phase. If the Resolver has a LAGGING input to output phase shift an R-C lagging phase shift network (low pass network) would be required. The resistor group D would need a capacitor in parallel and if no attenuation is required the resistor can be omitted.

The Reference Phase Lead can be calculated by the following formula;

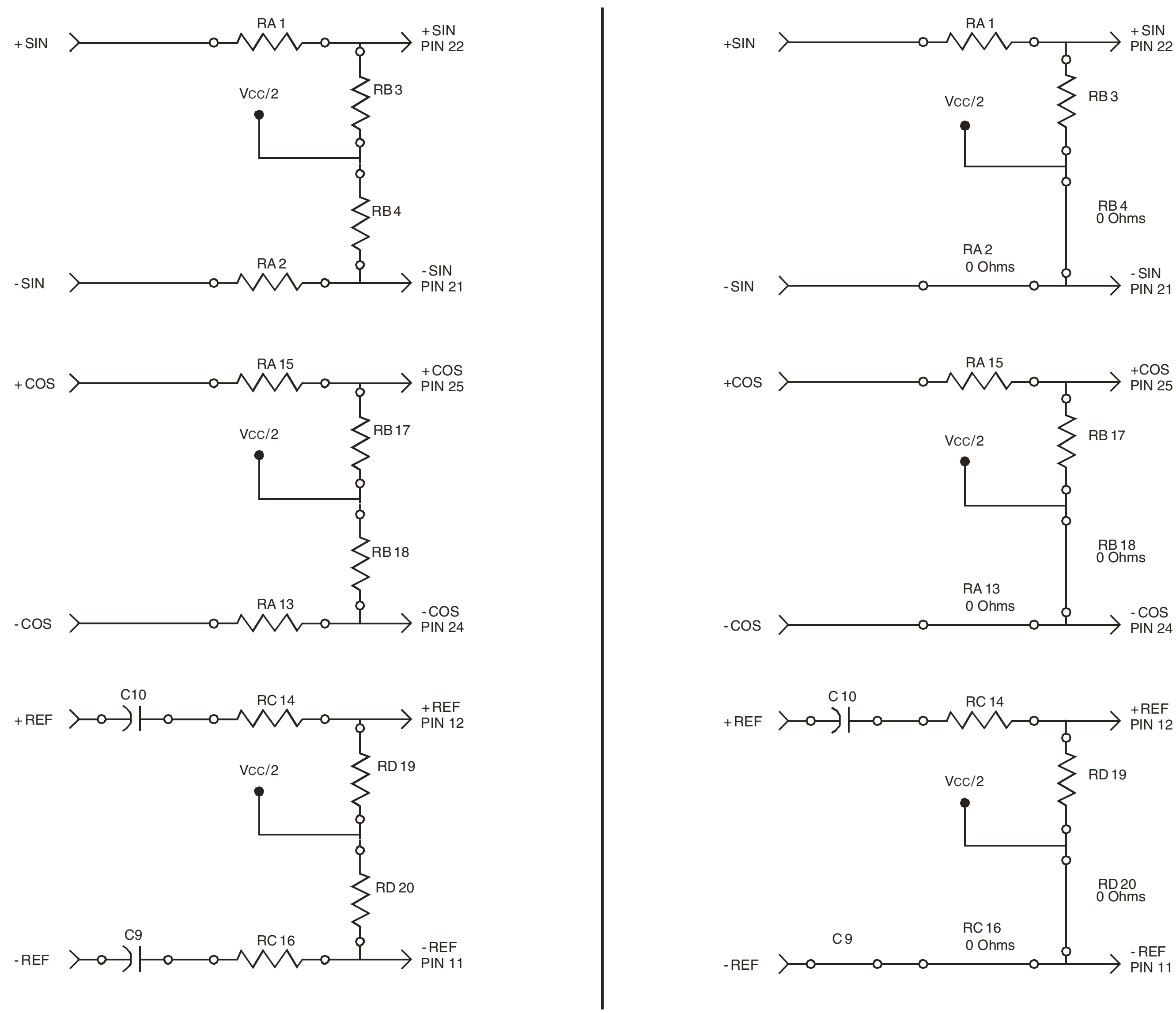
$$\text{Phase angle} = \text{ArcTan} \frac{1}{\dfrac{6.28 \times (RC + RD) \times C}{F_{REF}}}$$

F_{REF} is the reference frequency for the Reference signal being applied to the RDC Reference input.

When selecting component it would be easiest to select the capacitor values C9 and C10 (Ceramic Capacitors) that should be matched as close as possible. After first selecting the capacitor use the following formula to select the resistors.

$$RC + RD = \frac{1}{(\text{Tan (Phase Angle)}) \times FREF \times 6.28 \times C}$$

Note the C-R phase lead circuit on the input to the Demodulator (pins 15 & 16) should be considered when calculating the total system phase compensation. This phase lead adds to the phase lead developed by the Resolver.



Differential Input Configuration

Single-Ended Input Configuration

Figure 1 – Input Signal Conditioning