Mixed-Signal Circuit Design Using Ground-Signal-Ground Technology

06

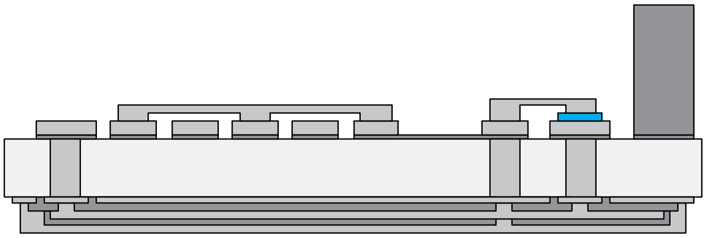
MIC Technology
Corporation

The increased use of mixed-signal circuit designs combining rapidly switched digital control signals or power supply signals with RF/microwave circuitry has created a hostile crosstalk environment in today's microelectronic assemblies. MIC Technology has developed ground-signal-ground (GSG) multi-layer technology for use on PIMICs™ (Passive Integrated Micro-electronic Interconnect Circuitry) to specifically address this problem. This unique process enables the routing of shielded signals on the backside of PIMIC-AI and MSI circuits without disrupting RF ground plane continuity, effectively doubling the available routing space within a design. In addition to high-density shielded interconnect, GSG substrates permit full use of MIC's passive integrated component processes on the top surface of the circuit. For ease of use, MIC Technology provides low cost autorouting and artwork generation for backside GSG layers from an initial customer layout and netlist.

Product Description and Use

Ground-Signal-Ground substrates get their name from their physical construction which places an insulated signal layer between two ground planes on the back surface of a ceramic substrate as shown in Figure 1. Thin film deposition and lithography techniques used to manufacture this product line result in reliable structures which benefit from fine-line definition and excellent surface qualities. The minimal thickness of each layer results in a final substrate height only marginally greater than the starting thickness, allowing GSG circuits to be conveniently assembled adjacent to standard PIMIC™ substrates without height discontinuities. The presence of two capacitively-coupled ground planes around the embedded signal layer, meanwhile, quiets signal noise and frees up area on the top surface of the substrate for additional trace routing. Unique grounding techniques maintain RF ground plane continuity, making the two separated shield layers act as a single ground. MIC Technology's proprietary filled vias are used to connect signal lines between the top and bottom surfaces of the substrate as well as to provide grounded die mounting sites where required. On the top surface of the substrate, standard PIMIC™ layout techniques apply, permitting fine-line DC or microwave structures, airbridges, capacitors, and other passive elements as discussed in MIC's introductory guide to PIMIC™ technology.

Figure 1: PIMIC™ Circuit Using Ground-Signal-Ground Interconnect



Applications which benefit from this product include advanced, high-density T/R modules with digital control circuitry, balanced power amplifiers, and low noise amplifiers. The balanced power amplifier portion of T/R modules or stand-alone power modules often have FET bias connections and control lines running in close proximity to microwave transmission lines and Lange couplers. In these situations, high-current pulses on the drain lines or rapidly switching gate modulation signals can induce significant noise on adjacent conductor traces. This problem is often magnified by the fact that bias connections to the active die must jump over RF lines to get to the FET or MMIC wirebond sites. Using ground-signal-ground technology, the circuit engineer routes noisy drain lines or sensitive bias/control lines on the back side of the substrate beneath RF structures, such as Lange couplers, existing on the top side of the circuit. Filled vias are strategically placed to access control signals where required, often in confined areas bordered by RF interconnections. The small footprint afforded with filled vias to access backside signals enables bond site placement which assures minimal crosstalk with local RF traces. Completed GSG circuits benefit, therefore, from enhanced integration density through surface-mounting of active die, passive component integration, reduced crosstalk, and packaging flexibility. Physical parameters of GSG technology are identified in Table 1.

Layout Guidelines

For customers wishing to route their own Ground-Signal-Ground circuits, rather than using MIC Technology's in-house capability, this section provides step-by-step layout rules. Ground-Signal-Ground substrates employ a structured design approach and a library of features to create circuits with standardized design characteristics. Careful adherence to these rules will result in an easily manufacturable, successful design.

For purposes of the following step by step layout description, the A-side of the substrate will be defined as the top surface of the circuit where RF trace routing occurs, while the B-side will be the bottom surface to which the package or carrier is attached.

Step 1: Layout A-Side Circuitry

Using MIC Technology's standard layout rules, create your DC/RF/Microwave circuit layout, including SI and/or AI features such as resistors, vias, capacitors, and air-bridges. A multilevel CAD system is helpful when doing this in order to segregate design features. A-side layers should be named using the conventions of Table 2. Illustrations in the following sections will highlight B-side features and assume the user has met design guidelines for A-side circuitry.

Table 1: Ground-Signal-Ground Physical Characteristics

Parameter	Value	Description
Substrate Material	Alumina BeO	10-25 mils thick (250-625 µm) 15-25 mils thick (375-625 µm)
Layers, Front Side	1-6	Resistors, Conductors, Capacitors, Inductors, Air-Bridges, HDDI
Layers, Back Side	5	M1 = M3 = Ground P1 = P2 = Insulator M2 = Signal
Interconnection Method. Front to Back	Filled Vias	Compliant to Requirements of Filled Via Design Guide
B-Side Line/Space, Min.	2.5 mils (62.5 µm)	
Insulator Material	Polyimide	7µm thickness, Nominal
Breakdown Voltage	100V	Minimum
Signal Trace Capacitance	.01pf/mil^2 (17pf/mm^2)	Minimum
Metallization System	TiW/Au	Pd or Ni Barrier Layers Optional
Conductor Plane Sheet Resistance	5mΩ/sq	Typical

Table 2: A-Side Layer Names

Layer Name	Description
TEXT	Dimensions, Fabrication Notes, Probe Points
MACHINE	Circuit Outline, Via Locations, Laser Cuts
RESISTOR	TaN or NiCr Resistors
COND1	Base Level Conductor Traces
COND2	Selective High Conductivity Traces
AB	Second-Level Conductor Traces or Air-Bridges
DIELECTRIC	Poly or SiN Dielectrics

Step 2: Create a Library of Elements

The B-side of a ground-signal-ground circuit uses a number of features to connect signals, grounds, and ground planes. These library elements utilize several of the 5 CAD layers identified previously in Table 1 which comprise the multi-level backplane. Table 3 below identifies these elements, their purpose, and the layers used to construct them. Figure 2 illustrates the details of each feature while subsequent steps describe the detailed dimensional requirements and placement of each element. Note that Figures 3 and 4 indicate dimensional requirement for signal and ground connections using 14 mil diameter vias. When larger vias are used, as required by thicker substrate materials, the signal and ground via elements in these figures are increased in size as indicated. By creating and saving individual cells of library elements as the design progresses, subsequent edits and new designs are simplified.

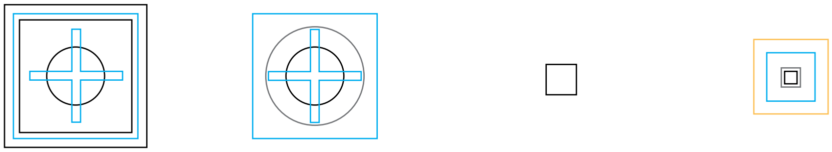
Step 3: Place Signal Via Stacks

Signal traces to be routed on the B-side of the substrate originate from signal vias which connect to the circuit's A-side. Your initial A-side layout will have determined these via locations enabling proper placement of B-side signal vias stacks. Three CAD layers are used to create these stacks consisting of clearance openings and capture pads. Locate all of the signal vias in your design and center a signal via stack over each one. Remember to use a via stack appropriate for your via diameter. Specifically, 10 and 15 mil thick substrates use the structure shown in Figure 3 while 20 mil thick substrates add 2 mils (50 µm) to all dimensions and 25 mil substrates add 6 mils (150 µm) to all dimensions as indicated in Table 4. For purposes of clarity, note that the M2 capture pad has a cross-shaped area removed from its center. This feature must also enlarge accordingly for larger via sizes. Although the capture pads in this structure have been identified as squares, circular pads may be used at the expense of larger CAD files and slightly costlier masks.

Table 3: Ground-Signal-Ground Library Elements

Library Element	Description	CAD Layers Used
Signal Via	Isolate signal connections from ground plane and transition to signal plane	M1,P1,M2
Ground Via Splice	Connect filled ground via to ground plane #2	P1,M2,P2
Ground Stitch	Connect ground plane #1 to ground plane #2	P1,M2,P2
Poly Stitch	N/A	M1

Figure 2: Ground Signal Ground Library Elements



Signal Via

Ground Via Splice

Poly Stitch

Ground Plane Stitch

Figure 3: Signal Via Stack for 10 and 15 mil Thick Substrates

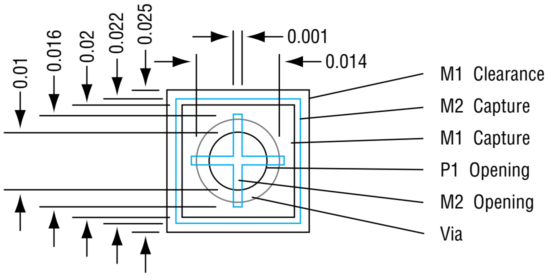


Table 4: Signal Via Dimensional Summary

CAD FEATURE	Feature Size w /14 mil Vias (mils)	Feature Size w /16 mil Vias (mils)	Feature Size w /20 mil Vias (mils)
Substrate Thickness	10 or 15	20	25
M1 Capture Pad	20 x 20	22 x 22	26 x 26
M1 Clearance Area	25 x 25	27 x 27	31 x 31
P1 Opening (diameter)	10	12	16
M2 Capture Pad	22 x 22	24 x 24	28 x 28

Step 4: Create B-side Layer Pullbacks

Each B-side layer has a specific pullback requirement from the edge of the substrate, with successive layers being pulled back farther from the circuit edge. When completed, this results in a pyramid layering effect. Now that signal vias have been placed, the minimum area requiring polyimide deposition has been defined. The user should identify the substrate edge as well as the edges of any internal laser cutouts and then draw each layer outline per the rules of Table 5. All of the layers except for M2 fully cover the backside of the substrate so an actual layer outline is required for each of those layers. Note that the M3 layer artwork is solely defined by the creation of its outline.

The M2 layer does not require a specific outline, but rather, conductor traces may not extend beyond the pullback limit.

Although the M1 layer effectively covers the entire backside of the circuit, it may be desirable in some cases to limit the coverage area of layers P1 through M3 to any area only sufficiently large to cover the M2 signal traces, leaving the M1 ground plane exposed where no routing exists. This approach is acceptable for epoxy or solder-based circuit attachment with proper preform thickness. To use partial backside coverage, keep the pullback relationships between P1, M2, P2, and M3 the same as in Table 5, but allow the M1 to P1 pullback relationship to grow above the 4 mil baseline value.

Step 5: Overlay Ground Via Splices

Filled ground vias located within the polyimide coverage area are normally connected through the polyimide layers to the second ground plane (M3) to form a spliced ground via connection. In a manner similar to the signal via, locate the position of each ground via and center the appropriate ground via splice over each one as shown in Figure 4. For larger vias in thicker material, enlarge the via splice dimensions per Table 6.

Table 5: B-Side Pullback Requirements

Layer	Pullback From Circuit/Cutout Edges	Pullback From Previous Layer
M1	2 mils (50 µm)	N/A
P1	6 mils (150 µm)	+4
M2	10 mils (250 µm)	+4
P2	8 mils (200 µm)	-2
M3	4 mils (100 µm)	-4

Figure 4: Ground Via Splices for 10 and 15 mil Substrates

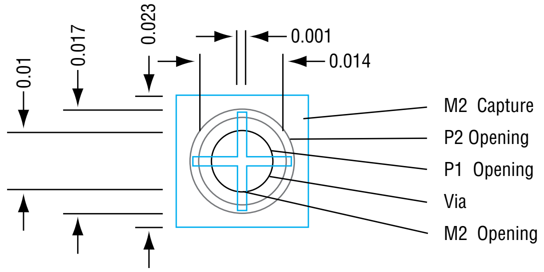


Table 6: Ground Via Splices Dimensional Summary

CAD FEATURE	Feature Size w /14 mil Vias (mils)	Feature Size w /16 mil Vias (mils)	Feature Size w /20 mil Vias (mils)
Substrate Thickness	10 or 15	20	25
P1 Opening (Diameter)	10 x 10	12 x 12	16 x 16
M2 Capture Pad	23 x 23	25 x 25	29 x 29
P2 Opening (Diameter)	17 x 17	19 x 19	23 x 23

Step 6: Create Poly-Stitching

Now that the via structures have been placed, the designer must add polyimide stitches to all regions where P1 overlays M1. Two types of stitching are used to accomplish this; perimeter stitching and interior stitching. Perimeter stitching consists of a single row of 5 mil square openings in the M1 ground plane located on 15 mil centers. These stitches completely encircle the polyimide area and are pulled back from the polyimide edge by a predefined distance.

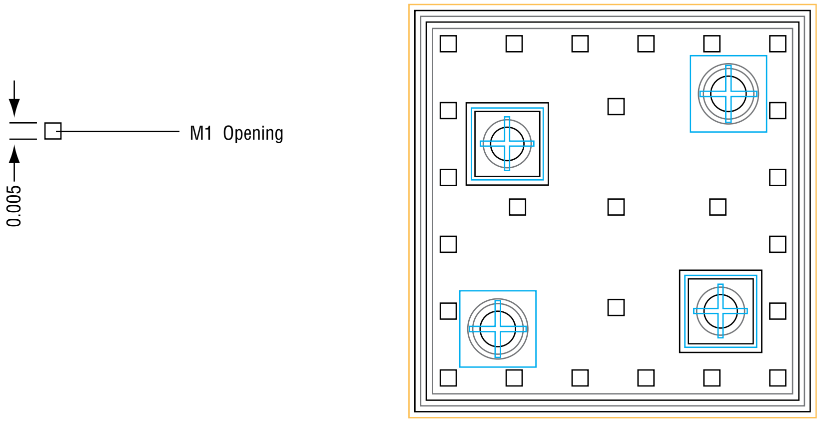
Interior stitching consists of a matrix of 5 mil square openings in the M1 layer spaced on 30 mil centers across the entire polyimide interior. In each case, the stitch openings are deleted where layout conflicts exist, including over “keep-out” areas, filled vias and etched features.

“Keep-out” areas on the B-side of the circuit are defined as those areas directly below critical RF structures routed on the A-side of the circuit, plus a buffer region. Prior to poly-stitch placement, these areas should be outlined on the circuit B-side, including a 20 mil (per side), buffer area. Poly stitches left within this region after first-pass stitch placement should be deleted to enhance RF ground-plane performance. Table 7 defines the critical aspects of the two stitch types while the visual results of layout steps to date, including poly-stitch placement, are shown in Figure 5.

Table 7: Poly-Stitch Specifications

Stitch Type	Size mils (µm)	Pitch, (C to C) mils (µm)	CAD Layer	Pullback from P1 Layer, Edge to Edge
Perimeter	5 x 5 (125 x 125)	15-20 (375-500)	M1	8 mils (200 µm) min
Interior	5 x 5 (125 x 125)	20-50 (500-1250)	M1	40 mils (1000 µm) max

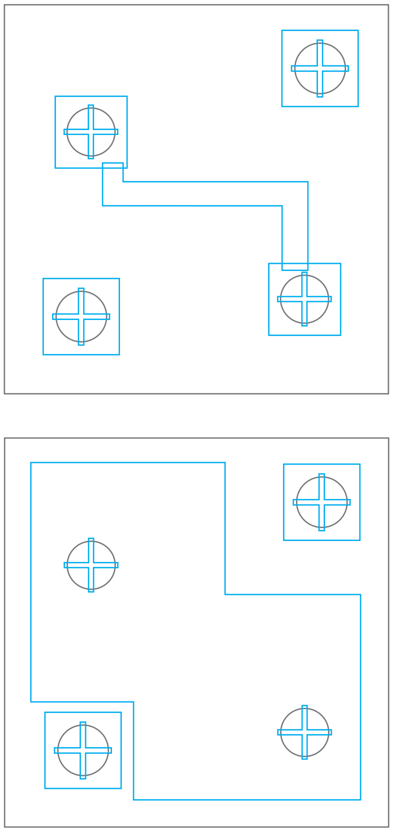
Figure 5: Ground-Signal-Ground Layout Prior to Trace Routing



Step 7: Route B-Side Traces

Now that vias and stitching have been properly configured, signal traces may be routed between signal vias using conductor patterns on the M2 layer. In general, low current signals are routed using trace widths on the order of 5-15 mils (125-375µm) while high current lines often utilize large planes of metal occupying most of the M2 level. When possible, experience has shown that it is convenient to route the signal traces directly over the poly-stitching grid. This approach leaves maximal area for the ground plane splices applied in Step 8. In either case, the general requirements that must be met are to ensure that M2 metal is properly pulled back from the edge of the circuit per Table 5 and that a minimum 2.5 mil (62.5 µm) gap occurs between any other traces or pads located on M2. The completed conductor traces should overlap the signal via capture pads, drawn previously, by 1 mil (25 µm). In the case of a large area conductor plane, the trace will fully enclose the signal via. An example of individual trace routing is compared to large area routing in Figure 6.

Figure 6: Examples of Trace Routing Approaches



Step 8: Apply Ground Plane Stitching

In microwave circuits, it is particularly critical that the ground plane on the B-side be continuous and intimately connected with the package mounting surface. The final step in GSG layout ensures that the 2 ground planes (M1 and M3) behave as one in the final assembly by connecting the two planes together at regular intervals. A ground stitch consists of P1 and P1 openings with an M2 capture pad. Assuming that signal traces have been routed over the poly-stitch grid as recommended in Step 7, a similar 30 mil grid of ground plane stitches may be offset from the poly-stitch grid by 15 mils in the X and Y axes. Additional specifications for ground stitches are summarized in Table 8 and illustrated in Figure 7. If your design does not route signal traces on the poly-stitch grid, the ground stitches applied here should follow a general placement guideline of at least every 50 mils. In cases where a full plane of metal is used on M2 to carry high current signals, the plane must be punctuated with ground plane stitches at regular intervals, employing a 2.5 mil annulus to isolate the ground splice capture pad from the signal plane as illustrated in the completed designs of Figure 8.

Table 8: Ground Stitch Specifications

Parameter	Value mils (µm)	Comment
CAD Layers and Feature sizes mils (µm)	P1 = 2 x 2 (50 x 50) M2 = 8 x 8 (200 x 200) P2 = 3 x 3 (75 x 75)	See figure 5
Pitch (C to C)	30 (750) typical 50 (1250) maximum	Delete occurrences within 3 mils of Vias and M1 etched features.
Stitch to Circuit Edge	30 (750) typ.	50 mil max recommended
Ground Pad to Signal Trace Clearance, M2	2.5 (62.5) min.	Minimum, all sides

Figure 7: Ground Stitch Element

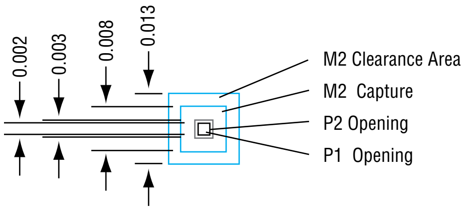
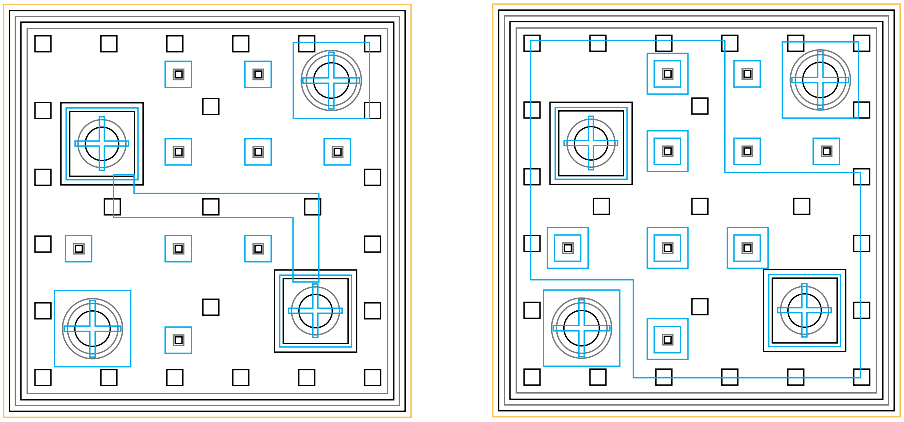


Figure 8: Completed GSG Layouts


Single Trace Connection

Large Area Connection

Step 9: Completing the Deliverable Package

At this point in the layout procedure, the GSG circuit is completed. A careful review of your design should be conducted at this time.

Finalizing an order for a ground-signal-ground circuit requires the customer to supply MIC Technology with a design package including:

- Mechanical drawings with notes ✔
- Environmental and assembly specifications ✔
- CAD files constructed with zero-width polylines ✔
- Netlist ✔
- Special probing requirements ✔

For those customers utilizing MIC Technology's in-house routing and layout capability, the netlist should also include current carrying requirements of each trace to enable proper choice of linewidths. MIC Technology will provide a completed layout package for these customers prior to fabrication of the circuit. Remember that a complete design input package will speed circuit fabrication and ensure a properly tested, spec-compliant product.

As with any MIC product, quality and customer satisfaction are guaranteed. Ground-Signal-Ground products are tested to meet or exceed all applicable military quality standards including MIL-STD-883D, Method 2032, Class H. Space-level (class K) testing is available as required.

Summary

Ground-Signal-Ground technology from MIC brings new options to designers of mixed signal circuits suffering from crosstalk problems and layout constraints. Using MIC Technology's PIMIC™ design literature, the engineer can easily route shielded signal lines in the presence of dense RF circuitry. By drawing upon the full complement of PIMIC™ tools, completed GSG circuits benefit from enhanced integration density through surface-mounting of active die, passive component integration, reduced crosstalk, and packaging flexibility.

NORTHEAST
797 Turnpike Street
North Andover, MA 01845
TEL: 508-687-9625
800-RING-MIC
FAX: 508-687-9721

SOUTHWEST
556 N. Diamond Bar Blvd.
Suite 303
Diamond Bar, CA 91765
TEL: 909-861-5055
FAX: 909-861-5598

SOUTHEAST
2910 Bay To Bay Blvd.
Suite 300
Tampa, FL 33629
TEL: 813-831-0494
FAX: 813-831-2871

EUROPE
MIC Technology, Sarl
15 Rue Boudeville
Thibaud Center
31100 Toulouse, France
TEL: 33 (16) 61 43 04 37
FAX: 33 (16) 61 43 04 46