

Aeroflex Application Note

RadHard MSI Power Dissipation

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Background

The purpose of this application note is to review the power consumption of Aeroflex Colorado Springs radiation-hardened, CMOS, medium scale integration product line (RadHard MSI Logic). It is important to understand the components of power consumption as related to CMOS logic devices and how each influences the power consumed by the logic. To perform a thorough power analysis it is necessary to investigate both standby power consumption and “at frequency” power consumption. This application note develops the components of CMOS logic consumption and gives examples of a power analysis.

Aeroflex implements the RadHard MSI family in 1.2 μ m and 0.6 μ m CMOS technology. In a CMOS logic device, total power is composed of both a capacitive and resistive element. The resistive component accounts for input pull-up or pull-down resistors or load resistors (e.g., TTL load). The capacitive component reflects the power required to switch internal and external capacitance along with shoot through current. Shoot through current refers to the intrinsic current consumed during CMOS logic switching. For applications with long periods of switching inactivity, calculate the power dissipation using the formula $P = I_{DDQ} * V_{DD}$.

Resistive Power Component:

Resistor pull-up/pull-down current or TTL sink-current

$$P = P_{RDY} I_O V_O \quad (\text{eq. 1})$$

Capacitive Power Component:

Switching of load capacitance

$$P = C_L V_{DD}^2 f \quad (\text{eq. 2})$$

Switching of internal capacitance

$$P = C_{INT} V_{DD}^2 f \quad (\text{eq. 3})$$

Current spiking during switching (includes shoot through current)

$$P = \frac{1}{2} [V_{DD} I_{DD} (\text{MAX}) (t_{RISE} + t_{FALL})] f \quad (\text{eq. 4})$$

Where:

f (Hz) is the operating frequency

C_L (pF) is the load capacitance

C_{INT} (pF) is the internal capacitance

To make the power dissipation calculations easier, combine the power equations to generate power constants for the three major logic components: internal gates, input buffers and output drivers.

Internal Gates	Input Buffers	Output Drivers
P_{INT} (eq 3 and 4)	P_{IB} (eq 3 and 4)	P_{OUT} (eq 2 and 4) C_L = 50 pF
8.25 (μW/gate/MHz)	10.0 (μW/buffer/MHz)	1.8 (8 mA) 2.0 (12 mA) (mW/driver/MHz)

Note: To scale the load capacitance the P_{OUT} needs to be scaled by the corresponding change in the load capacitance. If using a 100pF load the P_{OUT} for the 8mA driver would be (2*1.8 = 3.6 mW/driver/MHz) and the 12mA driver would be (2*2.0 = 4.0mW/driver/MHz). If the load was 30pF the mW/driver/MHz would need to be scaled by 0.6, etc.

Total Power Dissipation Equation:

To calculate total power dissipation for a device, sum the power that internal gates, input buffers, output drivers, and TTL sink current components consume.

$$P_{TOTAL} = [(N_{INT} * P_{INT} * f_{INT}) + (N_{IB} * P_{IB} * f_{IB}) + (N_{OUT} * P_{OUT} * f_{OUT}) + (N_{RES} * P_{RES} * P_{PRDY})]$$

Where:

- N_{INT} = Number of internal gates
- P_{INT} = Power per internal gate
- f_{INT} = Average operating frequency of the internal gates
- N_{IB} = Number of input buffers
- P_{IB} = Power per input buffer
- f_{IB} = Average operating frequency of the input buffers
- N_{OUT} = Number of output drivers
- P_{OUT} = Power per output driver
- f_{OUT} = Average operating frequency of the output drivers
- N_{RES} = Number of TTL output sink
- P_{RES} = Power for TTL output sink current
- P_{PRDY} = Percent duty cycle that output buffer is sinking TTL current

The power dissipation per switching output is calculated for a logic device by using the power dissipation equation P_{TOTAL}. Table 1 contains the switching power dissipation (P_{SW}) values for Aeroflex's RadHard MSI family for each switching output with units of mW/MHz. The values do not include the TTL output sink power contribution (N_{RES} * P_{RES} * P_{PRDY}).

Table 1.0 RadHard MSI Power Values for each Switching Output ^{1,2,3}.

MSI Part ID	Description	# In.	# Output	Gates	P _{sw} /Output
UTACTS/ACS00	Quad 2-Input NAND Gates	8	4 (8mA)	16	1.8 mW/MHz
UTACTS/ACS02	Quad 2-Input NOR Gates	8	4 (8mA)	16	1.8mW/MHz
UTACTS/ACS04	Hex Inverters	6	6 (8mA)	24	1.8mW/MHz
UTACTS/ACS08	Quad 2-Input AND Gates	8	4 (8mA)	16	1.8mW/MHz
UTACTS/ACS10	Triple 3-Input NAND Gates	9	3 (8mA)	24	1.8mW/MHz
UTACTS/ACS11	Triple 3-Input AND Gates	9	3 (8mA)	24	1.8mW/MHz
UTACTS/ACS14	Hex Inverting Schmitt Trigger	6	6 (8mA)	60	1.8mW/MHz
UTACTS/ACS20	Dual 4-input NAND Gates	8	2 (8mA)	32	1.8mW/MHz
UTACTS/ACS27	Triple 3-Input NOR Gate	9	3 (8mA)	12	1.8mW/MHz
UTACTS/ACS34	Hex Noninverting Buffers	6	6 (8mA)	0	1.8mW/MHz
UTACTS/ACS54	4-Wide AND-OR-INVERT Gates	8	1 (8mA)	28	1.8mW/MHz
UTACTS/ACS74	Dual D Flip-Flops with Clear & Preset	8	4 (8mA)	80	2.1mW/MHz
UTACTS/ACS85	4-Bit Comparators	11	3 (8mA)	202	2.3mW/MHz
UTACTS/ACS86	Quad 2-Input Exclusive OR Gates	8	4 (8mA)	16	1.8mW/MHz
UTACTS/ACS109	Dual J-K Flip-Flops	10	4 (8mA)	280	2.4mW/MHz
UTACTS/ACS132	Quad 2-Input NAND Schmitt Triggers	8	4 (8mA)	96	2.0mW/MHz
UTACTS/ACS138	3- to 8-Line Decoder/Demult.	6	8 (8mA)	100	1.9mW/MHz
UTACTS/ACS139	Dual 2-Line to 4-Line Decoder/Mult.	6	8 (8mA)	76	1.8mW/MHz
UTACTS/ACS151	1 of 8 Data Selectors/Multiplexers	12	2 (8mA)	194	2.6mW/MHz
UTACTS/ACS153	8-Line to 1-Line Multiplexer	12	2 (8mA)	112	2.3mW/MHz
UTACTS/ACS157	2- to 1-Line Non-inverting Multiplexer	10	4 (8mA)	140	2.0mW/MHz
UTACTS/ACS163	4-Bit Synchronous Counters	5	9 (8mA)	238	2.0mW/MHz
UTACTS/ACS164	8-Bit Shift Registers	4	8 (8mA)	260	2.0mW/MHz
UTACTS/ACS165	8-Bit Parallel Load Shift Registers	12	2 (8mA)	332	3.2mW/MHz
UTACTS/ACS169	4-Bit Up/Down Binary Counters	9	5 (8mA)	432	2.5mW/MHz
UTACTS/ACS190	Syn. 4-bit Up/Down Decade Counters	8	6 (8mA)	300	1.8mW/MHz
UTACTS/ACS191	Syn. 4-bit Up/Down Binary Counters	8	6 (8mA)	300	1.8mW/MHz
UTACTS/ACS193	Synchronous 4-bit Up/Down Counter	8	6 (8mA)	300	1.8mW/MHz
UTACTS/ACS240	Octal Three-State Buffer	10	8 (12mA)	40	2.0mW/MHz
UTACTS/ACS244	Octal Three-State Buffer/Line Drivers	10	8 (12mA)	8	2.0mW/MHz
UTACTS/ACS245	Octal Bus Transceivers, Three-State	2	16 (12mA)	24	2.0mW/MHz
UTACTS/ACS253	Dual 4-Input Multiplexers	12	2 (8mA)	120	2.3mW/MHz
UTACTS/ACS264	Look-Ahead Carry Generators	9	5 (8mA)	140	2.2mW/MHz
UTACTS/ACS273	Octal D-Flip-Flops with Clear	10	8 (8mA)	244	2.0mW/MHz
UTACTS/ACS279	Quadruple S-R Latches	10	4 (12mA)	112	2.3mW/MHz
UTACTS/ACS280	9-bit Parity Generators/Checkers	9	2 (8mA)	164	2.5mW/MHz
UTACTS/ACS283	4-Bit Binary Full Adders	9	5 (8mA)	174	2.3mW/MHz
UTACTS/ACS365	Hex Buffer/Line Driver, Three-State	8	6 (8mA)	16	1.8mW/MHz
UTACTS/ACS373	Octal Transparent Latches, Three-State	10	8 (8mA)	172	1.9mW/MHz
UTACTS/ACS374	8-Bit, D Type Flip-Flop, Three State	10	8 (8mA)	244	2.0mW/MHz
UTACTS/ACS540	Inverting Octal Buffer/line Driver	10	8 (8mA)	128	1.8mW/MHz
UTACTS/ACS541	Non-Inverting Octal Buffer/line Driver	10	8 (8mA)	4	1.8mW/MHz
UTACTS/ACS4002	Dual 4-Stage NOR Gates	8	2 (12mA)	32	2.2mW/MHz

Notes:

1. # In defines the number of inputs.
2. # Output defines the number of outputs and drive capability.
3. P_{sw}/Output is the power dissipation per switching output. The power values DO NOT include the resistive power component, typically a TTL load.

The power dissipation equation can be simplified to:

$$P_{TOTAL} = [(N_{INT} * P_{INT} * f_{INT}) + (N_{IB} * P_{IB} * f_{IB}) + (N_{OUT} * P_{OUT} * f_{OUT}) + (N_{RES} * P_{RES} * P_{PRDY})]$$

$$P_{TOTAL} = [(N_{SWO} * P_{SW}/Output * f) + (N_{RES} * P_{RES} * P_{PRDY})]$$

$$P_{TOTAL} = [(N_{SWO} * P_{SW}/Output * f) + (Loads * P_{RDY} * I_{OL} * V_{OL}) + (Loads * P_{RDY} * I_{OH} * V_{DP})]$$

Where: N_{SWO} is the number of switching outputs
 $P_{SW}/Output$ is the power dissipation per switching output in mW/MHz from Table 1
 f is the frequency that the outputs are switching at
 $V_{DP} = V_{DD} - V_{OH}$
 $Loads =$ the number of Loads that are being driven, $Loads = N_{SWO}$

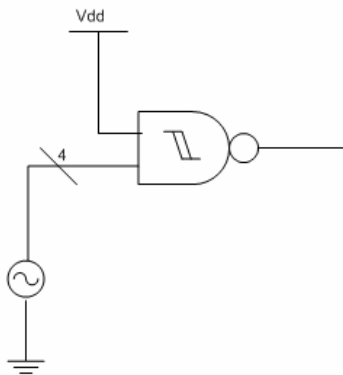
Next, an example power analysis is performed for a CMOS UT54ACS132 and a TTL UT54ACTS132 which are Quadruple 2-Input NAND Schmitt Triggers.

The ACS132 analysis assumes utilization of all 4 of the outputs switching at 80MHz, driving 4 loads low 40 percent of the time.

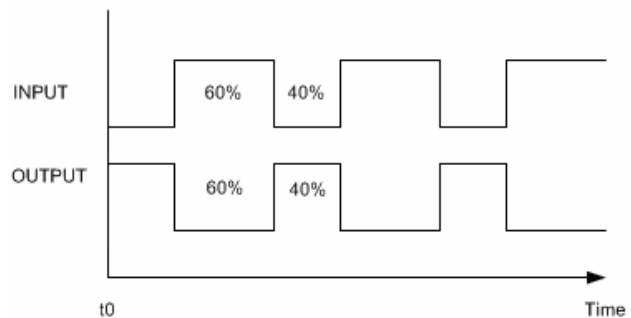
The ACTS132 analysis assumes utilization of 3 of the 4 outputs switching at 80MHz, driving 3 loads low 40 percent of the time.

Power Calculations:

The set up for the device is:



The input/output waveforms are:
 Input duty cycle is 60/40, output duty cycle is 40/60 due to inversion



UT54ACS132 Power

$$\begin{aligned}V_{DD} &= 5.0V & V_{OL} &= 0.25V \\N_{SWO} &= 4 & I_{OL} &= 100\mu A \\P_{SW} / \text{Output} &= 2.0mW / MHz & I_{OH} &= -100\mu A \\Loads &= 4 & V_{OH} &= 4.75V \\V_{DP} &= V_{DD} - V_{OH} = 5.0V - 4.75V = 0.25V\end{aligned}$$

$$\begin{aligned}P_{TOTAL} &= (4 * 2.0mW / MHz * 80MHz) + (4 * 0.4 * 100\mu A * 0.25V) + (4 * 0.6 * 100\mu A * 0.25V) \\P_{TOTAL} &= (640mW) + (0.04mW) + (0.06mW) = 0.6401W\end{aligned}$$

The increase in junction temperature can be calculated:

$$\begin{aligned}T_{INCREASE} &= \theta_{JC} * P_{TOTAL} \\T_{INCREASE} &= 20^\circ C / W * 0.6401W = 12.802 C^\circ\end{aligned}$$

UT54ACTS132 Power

$$\begin{aligned}V_{DD} &= 5.0V & V_{OL} &= 0.4V \\N_{SWO} &= 3 & I_{OL} &= 8mA \\P_{SW} / \text{Output} &= 2.0mW / MHz & I_{OH} &= -8mA \\Loads &= 3 & V_{OH} &= 3.5V \\V_{DP} &= V_{DD} - V_{OH} = 5.0V - 3.5V = 1.5V\end{aligned}$$

$$\begin{aligned}P_{TOTAL} &= (3 * 2.0mW / MHz * 80MHz) + (3 * 0.4 * 8mA * 0.4V) + (3 * 0.6 * 8mA * 1.5V) \\P_{TOTAL} &= (480mW) + (3.84mW) + (21.6mW) = 0.50544W\end{aligned}$$

The increase in junction temperature can be calculated:

$$\begin{aligned}T_{INCREASE} &= \theta_{JC} * P_{TOTAL} \\T_{INCREASE} &= 20^\circ C / W * 0.50544W = 10.1088 C^\circ\end{aligned}$$