

# UTMC Application Note

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## Modification List for the Intel EV80C196KD Evaluation Board

This application note describes modifications that must be made to the Intel EV80C196KD Evaluation Board so that it will work with the UTMC UT80CRH196KD Microcontroller. Each modification has been verified to work properly with the Intel device installed. This modification list is broken into the following categories:

1. Parts List (Describes the required hardware to complete the board modifications)
2. Modification Instructions
3. Jumper Settings (Describes how specific jumpers should be configured)

### Parts list:

<u>Quantity:</u>	<u>Description:</u>
1	20.00Mhz digital oscillator
13	5 Kohm leaded resistors
1	UTMC supplied High-Byte monitor PROM
1	UTMC supplied Low-Byte monitor PROM

### Modification Instructions:

1. Remove C4, C5 and X1 (20mhz crystal). Install a digital 20MHz oscillator to the pad where X1-right was connected. Short the power pin of the oscillator to R1-right. Short the ground pin of the oscillator to C4-left. Short a jumper wire from C4-left to X1-left. This will ground pin 66 on the processor. If you modify this board and use the Intel 80C196KD, you must remove this jumper to ensure proper operation.
2. Lift (isolate) U15-9. Connect U15-11 to U15-9 pad. In the beta version of the UT80CRH196KD device  $\overline{\text{BHE}}$  is not valid until  $\overline{\text{WR}}$  goes valid. This modification allows  $\overline{\text{BHE}}$  to be used, as well as allowing proper operation of the Intel device.
3. Remove C15. (Pin 37 is the  $\overline{\text{EDACEN}}$  digital input to the UT80CRH196KD).
4. Remove the C2 array of capacitors. (Port 0 is a digital signal port).
5. Replace U1 and U8 with the UTMC supplied monitor PROMs. U1 is the high byte PROM, and U8 is the low byte PROM.
6. UTMC suggests defining Port0 inputs by tying ACH0-ACH7 to ANGND (actually  $V_{SS}$ ) through 5K Ohm pulldown resistors (the UT80CRH196KD drives these as outputs during EDAC writes, do not directly connect these pins to power or ground).

\*ACH0: JP1-2 => 5K resistor => JP1-1  
\*ACH1: JP1-6 => 5K resistor => JP1-5  
\*ACH2: JP1-8 => 5K resistor => JP1-7  
\*ACH3: JP1-12 => 5K resistor => JP1-11  
ACH4: JP1-14 => 5K resistor => JP1-13  
ACH5: JP1-18 => 5K resistor => JP1-17  
\*ACH6: JP1-20 => 5K resistor => JP1-19  
ACH7: JP1-24 => 5K resistor => JP1-23

Note: The jumper pins JP1-1, 5, 7, 11, 13, 17, 19, and 23 are connected to  $V_{SS}$ .

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\* => These signals are driven by the UT80CRH196KD when the  $\overline{\text{EDACEN}}$  is active

7. UTMC suggests defining Port2(4:1) by tying to  $V_{SS}$  through 5K Ohm resistors.

P2.1: JP2-20 -> 5K resistor -> JP2-19

P2.2: JP2-22 -> 5K resistor -> JP2-21

P2.3: JP2-24 -> 5K resistor -> JP2-23

P2.4: JP2-26 -> 5K resistor -> JP2-25

Note: The jumper pins JP2-19, 21, 23, and 25 are connected to  $V_{SS}$ .

### **Jumper Settings:**

1. E6: A-B => U5-14 requires a connection to GND.  
(CDE pin on Intel part,  $V_{SS}$  pin on the UT80CRH196KD part).
2. E4: A-B => U5-13 requires a connection to  $V_{CC}$ .  
(Vref on Intel part,  $V_{DD}$  on the UT80CRH196KD part).
3. E2: A-B => U5-12 requires a connection to GND.  
(ANGND on Intel,  $V_{SS}$  on the UT80CRH196KD).
4. E19: removed. RXD driven by 80196, not the RS232 conn P2.
5. E3: Remove the jumper and install a 5K Ohm resistor (pulldown) between A-B.  
Defines U5-2 (EA on Intel, ECB5 on the UT80CRH196KD).
6. E7: B-C enables the NMI to be driven by the UART.
7. E16: A-B enables Port1 to drive the LEDs.
8. E20: B-C enables the reset to be driven by the UART
9. E21: B-C disables wait states. (Necessary for the CCB read at address 2018h)
10. E11: A-B enables the  $\overline{\text{HOLD}}/\overline{\text{HOLDA}}$  feature.
11. E9: A-B connects the A15 input of the monitor PROMs, which will be low for all monitor addresses.
12. Keep the default settings for the rest of the memory jumpers: E1, E5, E8, E10, E12-E15, E17, E18.